Fibocom

PERFECT WIRELESS EXPERIENCE

FM350-GL Hardware Guide _General

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Applicability Type

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Contents

1 Foreword 8

1.1 Introduction 8

1.2 Reference Standard 8

1.3 Related Document 9

2 Overview 10

2.1 Introduction 10

2.2 Specification 10

2.2.1 RF Characteristic 10

2.2.2 Key Features 11

2.3 CA Combinations 12

2.4 Application Block 14

2.5 Hardware Block Diagram 14

2.6 Antenna Configuration 15

3 Application Interface 16

3.1 M.2 Interface 16

3.1.1 Pin Map 16

3.1.2 Pin Definition 17

3.2 Power Supply 21

3.2.1 Power Supply 22

3.2.2 Logic Level 23

3.2.3 Power Consumption 23

3.3 Control Signal 26

3.3.1 Module Start-Up 27

3.3.1.1 Start-up Circuit 27

3.3.1.2 Start-up Timing Sequence 27

3.3.2 Module Shutdown 28

3.3.3 Module Reset 29

3.3.4 PCIe Link State 31

3.3.4.1 D0 L1.2 31

3.3.4.2 $D3_{cold}$ L2 32

3.3.5 Timing Application 33

3.4 PCIe Interface 33

3.4.1 PCIe Interface Definition 33

3.4.2 PCIe Interface Application 34
3.5 USIM Interface 36
3.5.1 USIM Pins 36
3.5.2 USIM Interface Circuit 36
3.5.2.1 N.C. SIM Card Slot 36
3.5.2.2 N.O. SIM Card Slot 37
3.5.3 USIM Hot-plug 38
3.5.4 USIM Design 38
3.6 Status Indicator 39
3.6.1 LED#1 Signal 39
3.6.2 WOWWAN# 40
3.7 Interrupt Control 40
3.7.1 W_DISABLE1# 41
3.7.2 BODYSAR 41
3.8 ANT Tunable Interface 41
3.9 Configuration Interface 42
4 Radio Frequency 43
4.1 RF Interface 43
4.1.1 RF Interface Functionality 43
4.1.2 RF Connector Characteristic 43
4.1.3 RF Connector Dimension 44
4.1.4 RF Connector Assembly 45
4.2 Operating Band 47
4.3 Transmitting Power 49
4.4 Receiver Sensitivity 51
4.4.1 Dual Antenna Receiver Sensitivity 51
4.4.2 Four Antenna Receiver Sensitivity 53
4.5 GNSS 55
4.6 Antenna Design 56
5 ESD Characteristics 58
6 Structure Specification 59
6.1 Product Appearance 59
6.2 Dimension of Structure 59
6.3 M.2 Interface Model 60

6.4 M.2 Connector 61
6.5 M.2 Card Assembly 63
6.5.1 Card Insertion 63
6.5.2 Mid-mount Connection with Single-Sided Module 64
6.5.3 Top-mount Connection with Single-Sided Module 64
6.6 Storage 65
6.6.1 Storage Life 65
6.7 Packing 65
6.7.1 Tray Package 65
6.7.2 Tray Size 67

1 Foreword

1.1 Introduction

The document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of FM350-GL (hereinafter referred to as FM350). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of FM350 modules and develop products.

1.2 Reference Standard

The design of the product complies with the following standards:

- 3GPP TS 38.300 V15.5.0: 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; NR and NG-RAN Overall Description; Stage 2
- 3GPP TS 38.521-1 V15.2.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Range 1 Standalone
- 3GPP TS 38.521-3 V15.2.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 3: Range 1 and Range 2 Interworking operation with other radios
- 3GPP TS 34.121-1 V8.11.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V11.13.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V14.0.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- PCI Express M.2 Specification Rev1.2

1.3 Related Document

- *FIBOCOM Design Guide_RF Antenna*

2 Overview

2.1 Introduction

FM350 is a highly integrated 5G Sub-6 WWAN module which uses M.2 form factor interface. It supports NR/LTE /WCDMA systems and can be applied to most cellular networks of mobile carrier in the world.

2.2 Specification

2.2.1 RF Characteristic

FM350 RF characteristic is shown in Table 2-1:

Table 2-1 RF characteristic

Operating Band	
NR Sub-6	n1/2/3/5/7/8/20/25/28/30/38/40/41/48[1)]/66/71/77/78/79
FDD-LTE	B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/29/30/32/66/71
TDD-LTE	B34/38/39/40/41/42/43/46/48
UMTS/HSPA+	B1/2/4/5/8
GNSS	GPS/GLONASS/Galileo/BDS/QZSS
Data Throughput	
Sub-6 SA	DL 4.67Gbps/UL 1.25Gbps
Sub-6 NSA	DL 3.74Gbps/UL 835Mbps
LTE	DL 1.6Gbps (CAT19)/UL 211Mbps(CAT18)
UMTS/HSPA+	DL UMTS: 384 kbps/UL 384 kbps
	DL DC-HSPA+: 42 Mbps (CAT24)/UL 11.5 Mbps (CAT7)
Modulation Characteristic	
NR Sub6 Modulation	3GPP Release 15 200MHz 2 DLCA, 256 QAM 200MHz 2 ULCA, 256 QAM 15KHz/30KHz SCS for FDD/TDD
LTE Modulation	3GPP Release 15 100MHz 5 DLCA, 256 QAM 40MHz 2 ULCA, 256 QAM
UMTS Modulation	3GPP Release 8
RF Characteristic	

HPUE	B41, n41/77[2)]/78/79
MIMO	NR DL 4x4 MIMO: n1/2/3/7/25/30/38/40/41/48/66/77/78/79
	NR UL 2x2 MIMO: n41/77/78/79
	LTE DL 4x4 MIMO: B1/2/3/4/7/25/30/34/38/39/40/41/42/43/48/66
SRS	n41/77/78/79
	1T2R/1T4R/2T4R
TX Switching	NR: n1/2/3/7/25/30/38/40/41/48/66/77/78/79
	LTE: B1/2/3/4/7/25/30/34/38/39/40/41/42/43/48/66
	UMTS/HSPA+: B1/2/4
Carrier Aggregation	
Sub-6 SA	DL 2CA, UL 2CA
Sub-6 NSA	DL LTE 5CA+ NR 1CA, LTE 3CA+ NR 2CA , UL LTE 2CA+ NR 1CA
LTE	DL 5CA, UL 2CA

2.2.2 Key Features

Table 2-2 Key features

Specification	
CPU	MTK T700, 7nm process, ARM Cortex-A55, up to 1.5 GHz
Memory	4Gb LPDDRX4+4Gb NAND Flash
Supported OS	Windows 10/Chrome (Linux/Android)
Power Supply	DC 3.135V to 4.4V, typical 3.3V
Temperature	Normal operating temperature: –10°C to +55°C
	Extended operating temperature: –30°C to +75°C[3)]
	Storage temperature: –40°C to +85°C
Physical Characteristics	Interface: M.2 Key-B
	Dimension: 30 x 52 x 2.3mm
	Weight: 8g
Interface	
Antenna Connector	WWAN Antenna x 4
	Support 4x4 MIMO
Function Interface	Dual SIM (one built-in eSIM), 1.8V/3V

	PCIe Gen3 x1
	USB 2.0 (For debug)
	USB 3.1 Gen1 (Reserved)
	W_Disable#
	BodySAR
	LED
	Tunable antenna
	I2C (Reserved)
	UART (Reserved)
Software	
Protocol Stack	IPV4/IPV6
AT Commands	3GPP TS 27.007 and 27.005
Firmware Update	PCIe
Other Feature	Multiple carrier
	Windows update

Note:

1) Disabled for FCC cannot certify currently, will enable in future after FCC can certify
2) n77 support HPUE only for FCC region application (cover 3.3–3.98GHz)
3) When temperature goes beyond normal operating temperature range of -10°C to +55°C, RF performance of module may be slightly off 3GPP specifications.

2.3 CA Combinations

DL CA Combinations		
2CA	Inter-band Intra-band	TBD

DL CA Combinations		
3CA	Inter-band Intra-band	TBD
4CA	Inter-band Intra-band	TBD
5CA	Inter-band Intra-band	TBD
NSA	TBD	TBD

2.4 Application Block

The peripheral applications for FM350 module are shown in Figure 2-1:

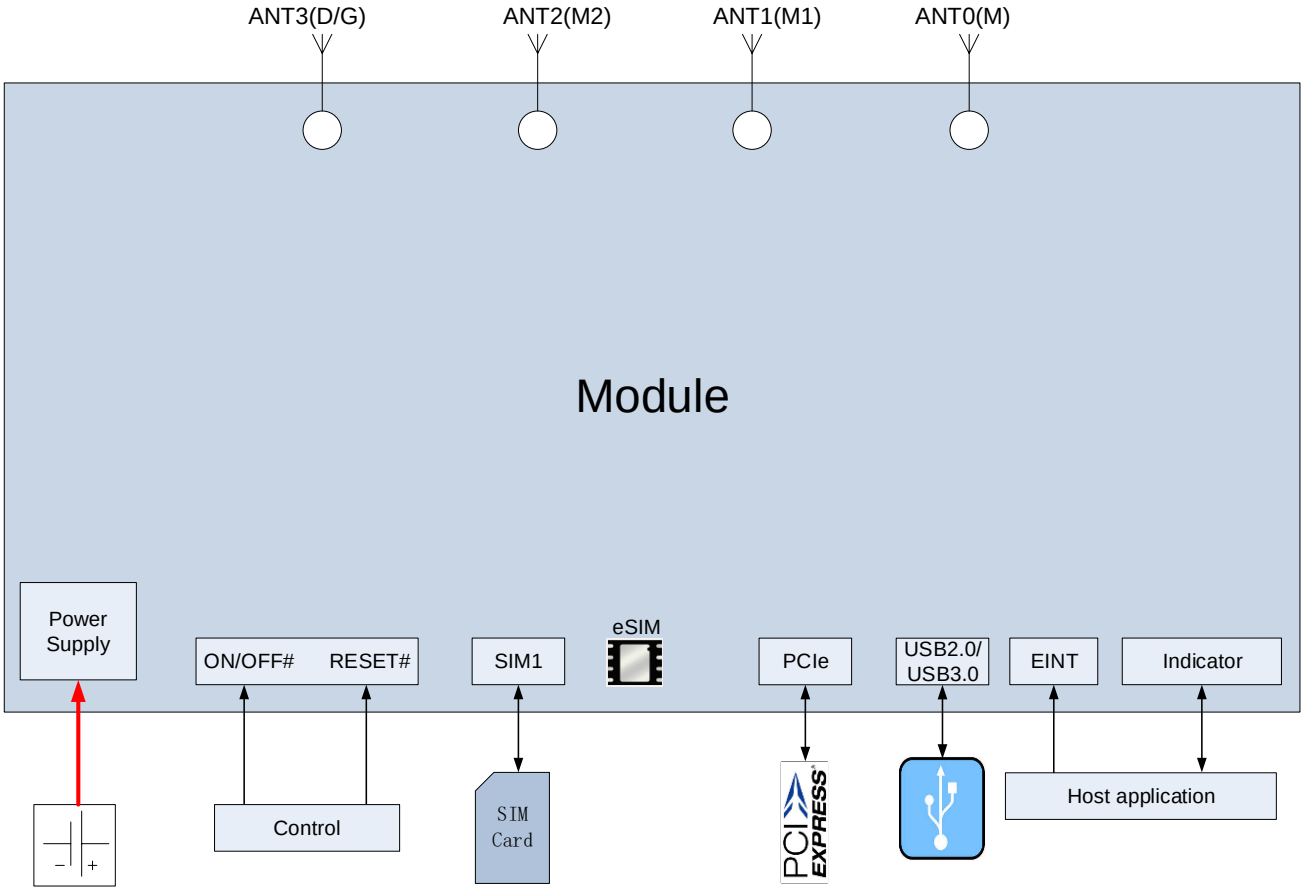

Figure 2-1 Application block

2.5 Hardware Block Diagram

The hardware block diagram in Figure 2-2 shows the main hardware functions of FM350 module, including base band and RF functions.

Baseband contains the followings:

- 5G NR/LTE/UMTS controller
- PMU
- MCP (NAND+LPDDR4 RAM)
- Application interface

RF contains the followings:

- RF Transceiver
- RF ET Power/PA
- RF PAMid/Front end
- RF SW
- RF Multi-plexer/Filter

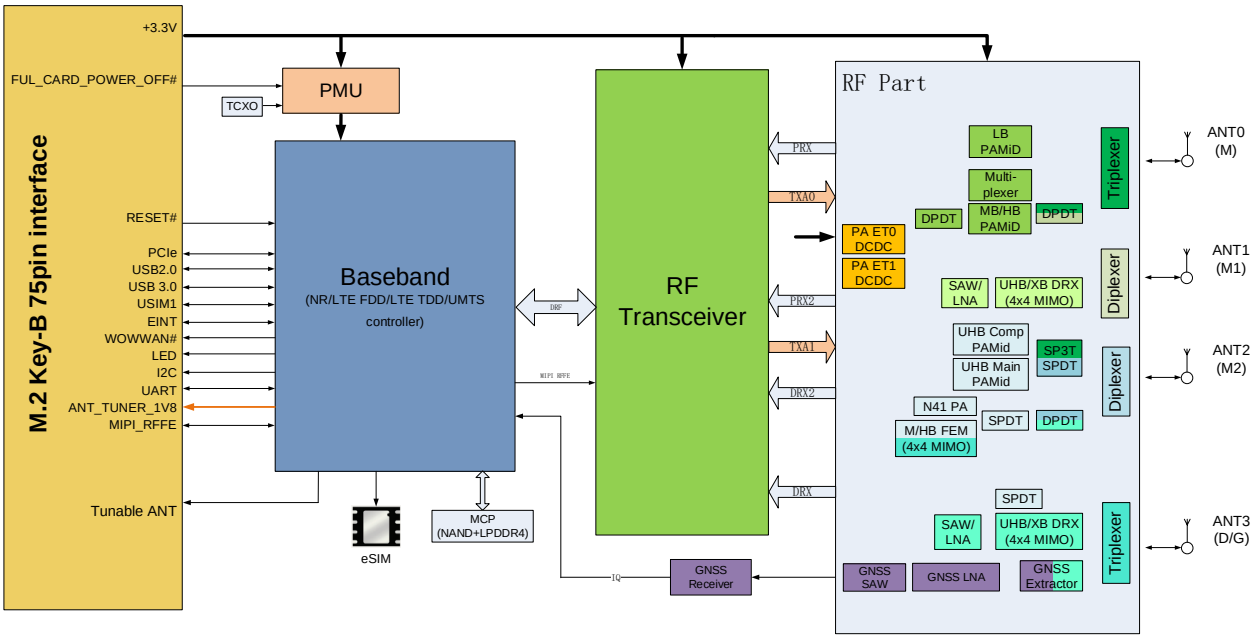

Figure 2-2 Hardware block diagram

2.6 Antenna Configuration

FM350 module supports four antennas and the configuration is as below table:

Antenna Connector	Function Description	Band Configuration	Frequency Range (MHz)
ANT0(M)	Main antenna port for TRX and SRS	All supported bands transmit & receive and SRS	617~5925
ANT1(M1)	Antenna port for RX and SRS	4x4MIMO supported bands receive and SRS	1805~5000
ANT2(M2)	Antenna port for TRX and SRS	Transmit, 4x4 MIMO receive and SRS	1452~5000
ANT3(D/G)	Diversity & GNSS ANT and SRS	All supported bands and GNSS receive, SRS	617~5925

3 Application Interface

3.1 M.2 Interface

The FM350 module applies standard M.2 Key-B interface, with a total of 75 pins.

3.1.1 Pin Map

74	+3.3V	CONFIG_2	75
72	+3.3V	VIO_CFG	73
70	+3.3V	GND	71
68	NC	CONFIG_1	69
66	SIM1_DETECT(1.8V)	RESET#(1.8V)	67
64	COEX_TXD(1.8V)	ANTCTL3(1.8V)	65
62	COEX_RXD(1.8V)	ANTCTL2(1.8V)	63
60	COEX3(1.8V)	ANTCTL1(1.8V)	61
58	RFE_RFFE_SDATA(1.8V)	ANTCTL0(1.8V)	59
56	RFE_RFFE_SCLK(1.8V)	GND	57
54	PEWAKE# (3.3/1.8V)	REFCLKP	55
52	CLKREQ# (3.3/1.8V)	REFCLKN	53
50	PERST# (3.3/1.8V)	GND	51
48	NC	PERp0	49
46	NC	PERn0	47
44	I2C_IRQ#(1.8V)	GND	45
42	I2C_SDA(1.8V,I2C Master/Slave)	PETp0	43
40	I2C_SCL(1.8V,I2C Master/Slave)	PETn0	41
38	NC	GND	39
36	UIM1_PWR	USB3.0-Rx+	37
34	UIM1_DATA	USB3.0-Rx−	35
32	UIM1_CLK	GND	33
30	UIM1_RESET	USB3.0-Tx+	31
28	UART_RX(1.8V,mux for DPR2/GPIO)	USB3.0-Tx−	29
26	W_DISABLE2#(3.3/1.8V)	GND	27
24	ANT_TUNER_1V8(1.8V, mux for GPIO)	DPR(3.3/1.8V)	25
22	UART_TX(1.8V, mux for ANT_TUNER_CFG/GPIO)	WOWWAN#(1.8V)	23
20	GPIO(1.8V)	CONFIG_0	21
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
10	LED1#(3.3V OD)	GND	11
8	W_DISABLE1#(3.3/1.8V)	USB D-	9
6	FULL_CARD_POWER_OFF#(3.3/1.8V)	USB D+	7
4	+3.3V	GND	5
2	+3.3V	GND	3
		CONFIG_3	1

Figure 3-1 Pin Map

Note:

Pin “Notch” represents the gap of the gold fingers.

3.1.2 Pin Definition

The pin definition is as below table:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
1	CONFIG_3	O	NC	NC, FM350 M.2 module is configured as the WWAN – PCIe Gen3, USB3.1 Gen1 interface type	-
2	+3.3V	PI	-	Power input	Power Supply
3	GND	-	-	GND	Power Supply
4	+3.3V	PI	-	Power input	Power Supply
5	GND	-	-	GND	Power Supply
6	FULL_CARD_ POWER_OFF#	I	PU	Power enable, module power on input, internal pull up(350KΩ)	3.3/1.8V
7	USB D+	I/O	-	USB data plus	0.3---3V
8	W_DISABLE1#	I	PD	WWAN disable, active low	3.3/1.8V
9	USB D-	I/O	-	USB data minus	0.3---3V
10	LED1#	OD	T	System status LED, output open drain, 3.3V	3.3V
11	GND	-	-	GND	Power Supply
12	Notch			Notch	
13	Notch			Notch	
14	Notch			Notch	
15	Notch			Notch	
16	Notch			Notch	
17	Notch			Notch	
18	Notch			Notch	
19	Notch			Notch	
20	GPIO	I/O	PD	GPIO. Reserved	1.8V
21	CONFIG_0	O	NC	GND, FM350 M.2 module is configured as the WWAN – PCIe Gen3, USB3.1 Gen1 interface type	-
22	UART_TX	O	PD	UART TXD output, can mux as ANT_TUNER_CFG or GPIO. Reserved	1.8V

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
23	WOWWAN#	O	PD	Wake up host, Reserved	1.8V
24	ANT_TUNER_1V8	O	PD	1.8V power output for antenna tuner, can mux as GPIO. Reserved	1.8V
25	DPR	I	PD	Dynamic power reduction - Body SAR control signal (SAR_BACK_OFF)	3.3/1.8V
26	W_DISABLE2#	I	PD	GNSS disable, active low, Reserved	3.3/1.8V
27	GND	-	-	GND	Power Supply
28	UART_RX	I	PD	UART RXD input, can mux as DPR2 or GPIO. Reserved	1.8V
29	USB3.0_TX-	O	-	USB3.0 transmit data minus, reserved	-
30	UIM_RESET	O	PD	SIM reset signal	1.8V/3V
31	USB3.0_TX+	O	-	USB3.0 transmit data plus, reserved	-
32	UIM_CLK	O	PD	SIM clock Signal	1.8V/3V
33	GND	-	-	GND	Power Supply
34	UIM_DATA	I/O	PD	SIM data input/output	1.8V/3V
35	USB3.0_RX-	I	-	USB3.0 receive data minus, reserved	-
36	UIM_PWR	O	-	SIM power supply, 1.8V/3V	1.8V/3V
37	USB3.0_RX+	I	-	USB3.0 receive data plus, reserved	-
38	NC		-	NC	-
39	GND	-	-	GND	Power Supply
40	I2C_SCL	O	PU	I2C master clock	1.8V
41	PETn0	O	-	PCIe TX differential signals negative	-
42	I2C_SDA	I/O	PU	I2C master data	1.8V
43	PETp0	O	-	PCIe TX differential signals positive	-
44	I2C_IRQ#	I	PU	I2C interrupt request	1.8V
45	GND	-	-	GND	Power Supply
46	NC	-	-	-	-
47	PERn0	I	-	PCIe RX differential signals negative	-

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
48	NC	-	-	-	-
49	PERp0	I	-	PCIe RX differential signals positive	-
50	PERST#	I	PU	Asserted to reset module PCIe interface default. If module went into core dump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ)	3.3/1.8V
51	GND	-	-	GND	Power Supply
52	CLKREQ#	I/O	PD	Asserted by device to request a PCIe reference clock be available (active clock state) in order to transmit data. It also used by L1 PM Sub states mechanism, asserted by either host or device to initiate an L1 exit. Active low, open drain output and should add external pull up on platform	3.3/1.8V
53	REFCLKN	I	-	PCIe reference clock signal Negative	-
54	PEWAKE#	O	T	Asserted to wake up system and reactivate PCIe link from L2 to L0, it depends on system whether supports wake up functionality. Active low, open drain output and should add external pull up on platform	3.3/1.8V
55	REFCLKP	I	-	PCIe reference clock signal Positive	-
56	RFFE_SCLK	O	PD	MIPI interface tunable ANT, RFFE clock	1.8V
57	GND			GND	Power Supply
58	RFFE_SDATA	I/O	PD	MIPI interface tunable ANT, RFFE data	1.8V
59	ANTCTL0	O	PD	Tunable ANT CTRL0	1.8V
60	COEX3	I/O	PD	Wireless coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. COEX_EXT_FTA, Reserved	1.8V

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
61	ANTCTL1	O	PD	Tunable ANT CTRL1	1.8V
62	COEX_RXD	I	PD	Wireless coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. UART receive signal(WWAN module side), Reserved	1.8V
63	ANTCTL2	O	PD	Tunable ANT CTRL2	1.8V
64	COEX_TXD	O	PD	Wireless coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. UART transmit signal(WWAN module side), Reserved	1.8V
65	ANTCTL3	O	PD	Tunable ANT CTRL3	1.8V
66	SIM1_DETECT	I	PU	SIM1 detect, internal pull up(390KΩ), active high	1.8V
67	RESET#	I	PU	WWAN reset input, active low, internal pull up(350KΩ)	1.8V
68	NC	-	-	NC	-
69	CONFIG_1	O	GND	GND, FM350 M.2 module is configured as the WWAN – PCIe Gen3, USB3.1 Gen1 interface type	-
70	+3.3V	PI	-	Power input	Power Supply
71	GND	-	-	GND	Power Supply
72	+3.3V	PI	-	Power input	Power Supply
73	VIO_CFG	-	NC	Configuration of PCIe sideband signals power domain NC: support 1.8V/3.3V; GND: support 3.3V	-
74	+3.3V	PI	-	Power input	Power Supply
75	CONFIG_2	O	NC	GND, FM350 M.2 module is configured as the WWAN – PCIe Gen3, USB3.1 Gen1 interface type	-

Reset Value: The initial status after module reset, not the status when working.

H: High Voltage Level

L: Low Voltage Level

PD: Pull-Down

PU: Pull-Up

T: Tristate

OD: Open Drain

PI: Power Input

PO: Power Output

Note:

Digital IO pins cannot be connected to power directly.

The unused pins can be left floating.

3.2 Power Supply

The power interface of FM350 module as shown in the following table:

Pin	Pin Name	I/O	Pin Description	DC Parameter (V)		
				Minimum Value	Typical Value	Maximum Value
2, 4, 70, 72, 74	+3.3V	PI	Power supply input	3.135	3.3	4.4
36	UIM_PWR	PO	USIM power supply	-	1.8V/3V	-

The Power rating table is as below table:

Pin	Pin Name	I/O	Pin Description	Current Consumption Limit Max Avg (mA)
2, 4, 70, 72, 74	+3.3V	PI	Power supply input	3500
36	UIM_PWR	PO	USIM power supply	200

FM350 module uses PCIe interface, according to the PCIe specification, the PCIe Vmain should be used as the +3.3V power source, not the Vaux. The Vaux is the PCIe backup power source and it is not sufficient as the power supply. In addition, the DC/DC power supply other than PCIe ports should not be used as the external power cannot control the module status through the PCIe protocol.

3.2.1 Power Supply

The FM350 module should be powered through the +3.3V pins, and the power supply design is shown in Figure 3-2:

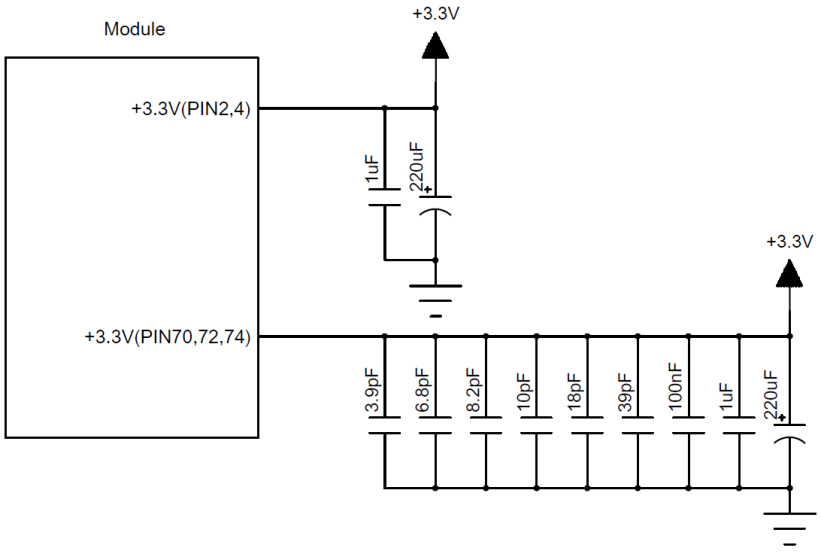

Figure 3-2 Power supply design

The filter capacitor design for power supply as shown in the following table:

Recommended capacitance	Application	Description
220uF x 2	Voltage-stabilizing capacitors	Reduce power fluctuations of the module in operation, requiring capacitors with low ESR. ● LDO or DC/DC power supply requires the capacitor of no less than 440uF ● The capacitor for battery power supply can be reduced to 100~200uF
1uF, 100nF	Digital signal noise	Filter out the interference generated from the clock and digital signals
39pF, 33pF	700/800, 850/900 MHz frequency band	Filter out low frequency band RF interference
18pF, 10pF, 8.2pF, 6.8pF, 3.9pF	1500/1800, 2100/2300, 2600MHz, 3500/3600/3700MHz, 5GHz	Filter out medium/high frequency band RF interference

The stable power supply can ensure the normal operation of FM350 module; and the ripple of the power supply should be less than 300mV in design. Module supports 5G NR Sub-6 download, when module operates with the maximum data transfer throughput, the peak current can reach to upper 3500mA. It

requests the power source voltage should not be lower than 3.135V, otherwise module may shut down or restart. The power supply requirement is shown in Figure 3-3:

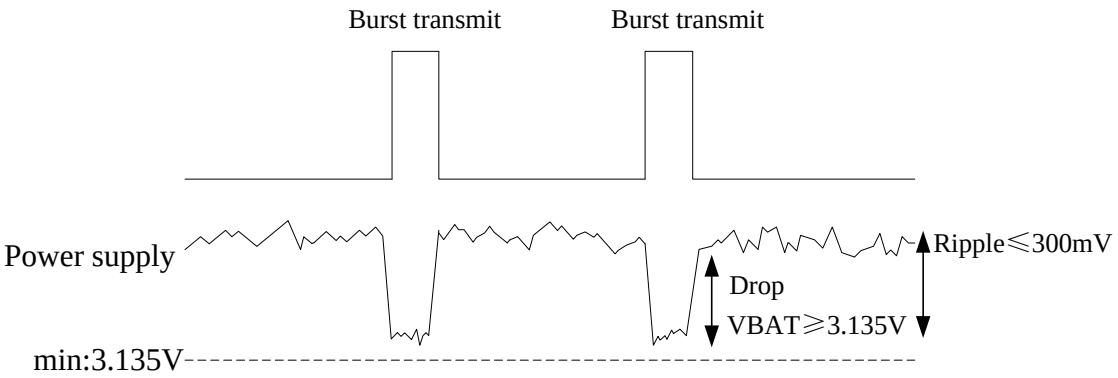

Figure 3-3 Power supply requirement

3.2.2 Logic Level

The FM350 module 1.8V logic level definition is shown in the following table:

Parameters	Minimum	Typical	Maximum	Unit
1.8V logic level	1.71	1.8	1.89	V
V_{IH}	1.3	1.8	1.89	V
V_{IL}@1mA	-0.3	0	0.3	V

The FM350 module 3.3V logic level definition is shown in the following table:

Parameters	Minimum	Typical	Maximum	Unit
3.3V logic level	3.135	3.3	3.465	V
V_{IH}	2.3	3.3	3.465	V
V_{IL}@1mA	-0.3	0	0.3	V

3.2.3 Power Consumption

In the condition of 3.3V power supply, the FM350 power consumption is shown in the following table:

Parameter	Mode	Condition	Average Current (mA)
I_{off}	Power off	Power supply, module power off	TBD
I_{Sleep}	WCDMA	DRX=8	TBD

Parameter	Mode	Condition	Average Current (mA)
	LTE FDD	Paging cycle #128 frames (1.28s DRx cycle)	TBD
	LTE TDD	Paging cycle #128 frames (1.28s DRx cycle)	TBD
	NR	Paging cycle #128 frames (1.28s DRx cycle)	TBD
	Radio Off	AT+CFUN=4, flight mode	TBD
$I_{WCDMA-RMS}$	WCDMA	Band1	TBD
		Band2	TBD
		Band4	TBD
		Band5	TBD
		Band8	TBD
$I_{LTE-RMS}$	LTE FDD	Band1	TBD
		Band2	TBD
		Band3	TBD
		Band4	TBD
		Band5	TBD
		Band7	TBD
		Band8	TBD
		Band12	TBD
		Band13	TBD
		Band14	TBD
		Band17	TBD
		Band18	TBD
		Band19	TBD
		Band20	TBD
		Band25	TBD
		Band26	TBD

Parameter	Mode	Condition	Average Current (mA)
		Band28	TBD
		Band30	TBD
		Band66	TBD
		Band71	TBD
	LTE TDD	Band34	TBD
		Band38	TBD
		Band39	TBD
		Band40	TBD
		Band41	TBD
		Band42	TBD
		Band43	TBD
		Band48	TBD
I_{NR-RMS}	NR	n1	TBD
		n2	TBD
		n3	TBD
		n5	TBD
		n7	TBD
		n8	TBD
		n20	TBD
		n25	TBD
		n28	TBD
		n30	TBD
		n38	TBD
		n40	TBD
		n41	TBD

Parameter	Mode	Condition	Average Current (mA)
		n48	TBD
		n66	TBD
		n71	TBD
		n77	TBD
		n78	TBD
		n79	TBD

Note：

The above data is the average value obtained by testing the sample for high/medium/low channels.

In 5CA/NSA combination, the FM350 power consumption is shown in the following table:

TBD

Note：

The data above is an average value tested on some samples at 25°C temperature.

3.3 Control Signal

The FM350 module provides two control signals for power on/off and reset operations. The pin is defined in the following table:

Pin	Pin Name	I/O	Reset Value	Function	Level
6	FULL_CARD_POWER_OFF#	I	PU	Module power on/off input, internal pull up(350KΩ) Power on: High/Floating Power off: Low	3.3/1.8V
67	RESET#	I	PU	WWAN reset input, active low, internal pull up(350KΩ)	1.8V
50	PERST#	I	PU	Asserted to reset module PCIe interface default. If module went into core dump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ)	3.3/1.8V

Note：

RESET# and PERST# need to be controlled by independent GPIO, and not shared with other devices on the host. RESET# and PERST# are sensitive signals, so they should keep away from RF interference and be protected by GND. It should be neither near PCB edge nor route on surface layer to avoid module abnormal reset caused by ESD.

3.3.1 Module Start-Up

3.3.1.1 Start-up Circuit

The FCPO# (FULL_CARD_POWER_OFF #) pin needs an external 3.3V or 1.8V pull up for booting up. AP (Application Processor) controls the module start-up. The recommended design is using a default PD port to control FCPO#. It also should reserve a 100K pull down resistor on AP side. The circuit design is shown in Figure 3-4:

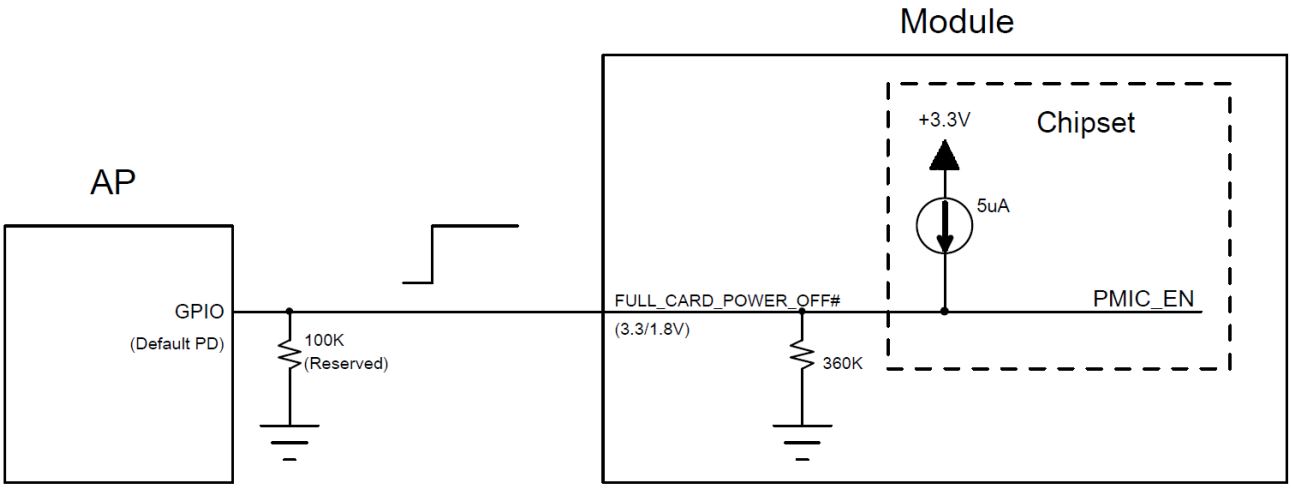

Figure 3-4 Circuit for module start-up controlled by AP

3.3.1.2 Start-up Timing Sequence

When power supply is ready, the PMU of module will power on and start initialization process by pulling high FCPO# signal. After about 20s, module will complete initialization process. The start-up timing is shown in Figure 3-5:

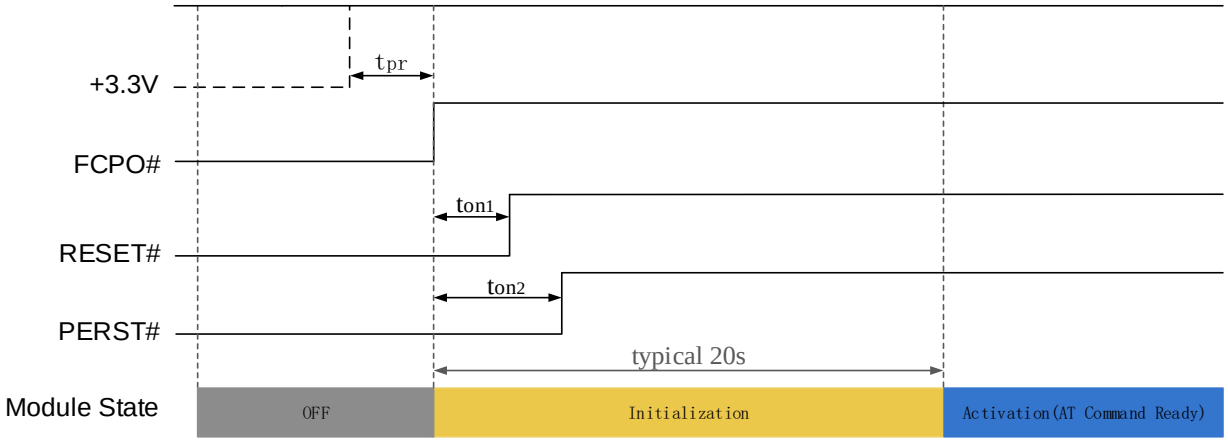

Figure 3-5 Timing control for start-up

Index	Min.	Recommended	Max.	Comments
t_{pr}	0ms	-	-	The delay time of power supply rising from 0V up to 3.3V.If power supply always ready, it can be ignored
t_{on1}	20ms	20ms	-	RESET# should be de-asserted after FCPO#
t_{on2}	50ms	100ms	-	The time delay of PERST# de-asserted after FCPO#, PERST# must always be the last to get de-asserted

The minimum detection time of PCIe link is about 23ms after PERST# de-asserted.

3.3.2 Module Shutdown

Module can be shut down by following control:

Shutdown Control	Action	Condition
Software	Sending AT+CPWROFF command	Normal shutdown (recommend)
Hardware	Pull down FCPO# pin	Only used when a hardware exception occurs and the software control cannot be used.

Module can be shut down by sending AT+CPWROFF command. When the module receives the software shutdown command, the module will start the finalization process (the reverse process of initialization), and it will be completed after t_{sd} time (t_{sd} is the time which AP receive OK of “AT+CPWROFF”, if there is no response, the max t_{sd} is 5s). In the finalization process, the module will save the network, SIM card and some other parameters from memory, then clear the memory and shut down PMU. The control timing is shown in Figure 3-6:

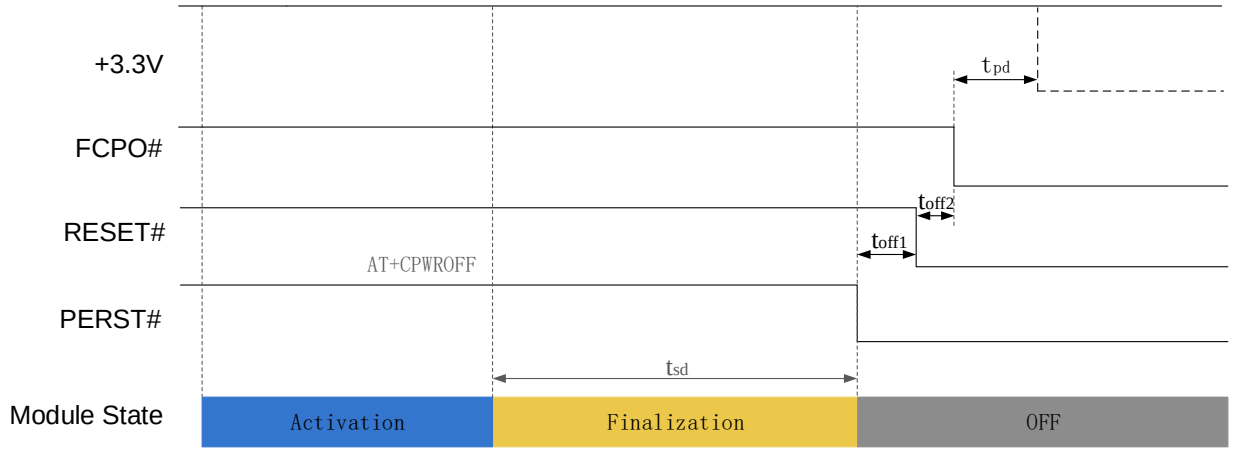

Figure 3-6 Shutdown timing control

Index	Min.	Recommended	Max.	Comments
t_{off1}	16ms	20ms	-	RESET# should be asserted after PERST#
t_{off2}	2ms	10ms	-	FCPO# should be asserted after RESET#
t_{pd}	10ms	100ms	-	+3.3V power supply goes down time. If power supply is always on, it can be ignored

3.3.3 Module Reset

The FM350 module can reset to its initial status by pulling down the RESET# signal for more than 2ms (10ms is recommended), and module will restart after RESET# signal is released. When customer executes RESET# function, the PMU remains its power inside the module. The recommended circuit design is shown in the Figure 3-7:

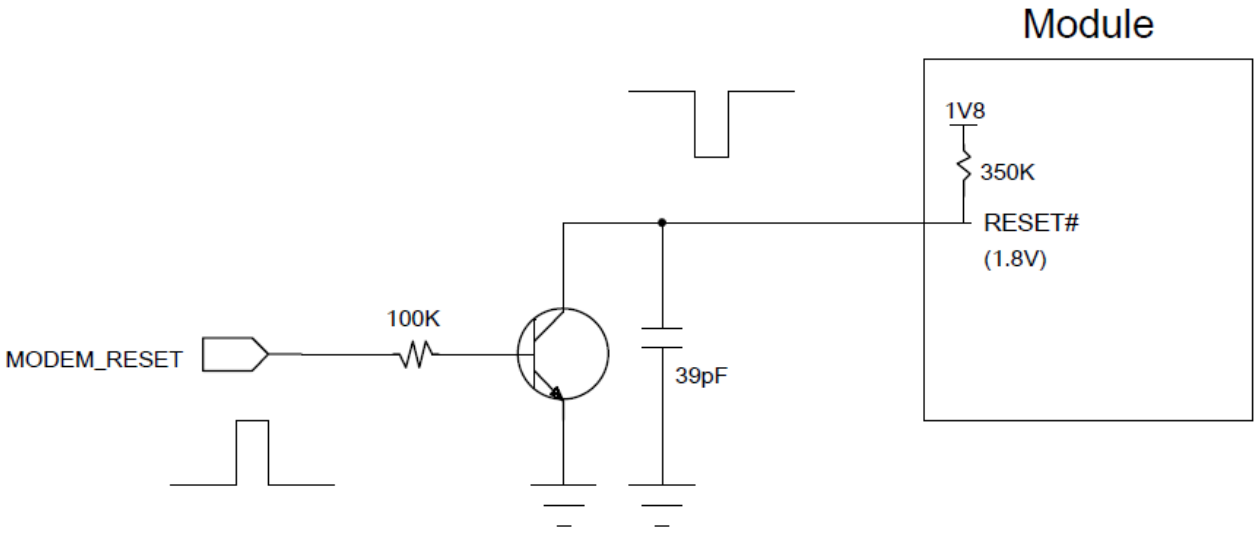

Figure 3-7 Recommended design for reset circuit

There are two reset control timings as below:

- Reset timing 1st in Figure 3-8, PMU of module internal always on in reset sequence, recommend using in FW upgrade and module recovery;
- Reset timing 2nd in Figure 3-9, PMU of module internal will be off in reset sequence (including whole power off and power on sequence, t_{sd} can refer section 3.3.2), recommend using in system warm boot.

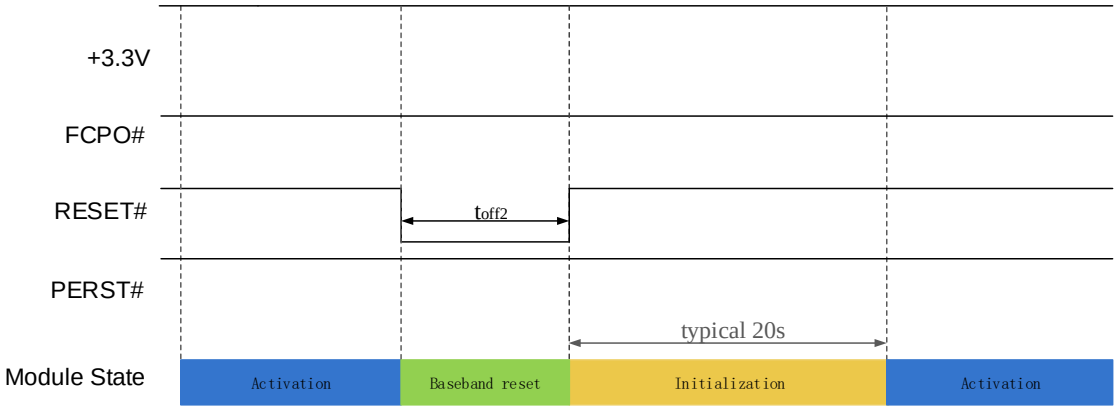

Figure 3-8 Reset control timing1st

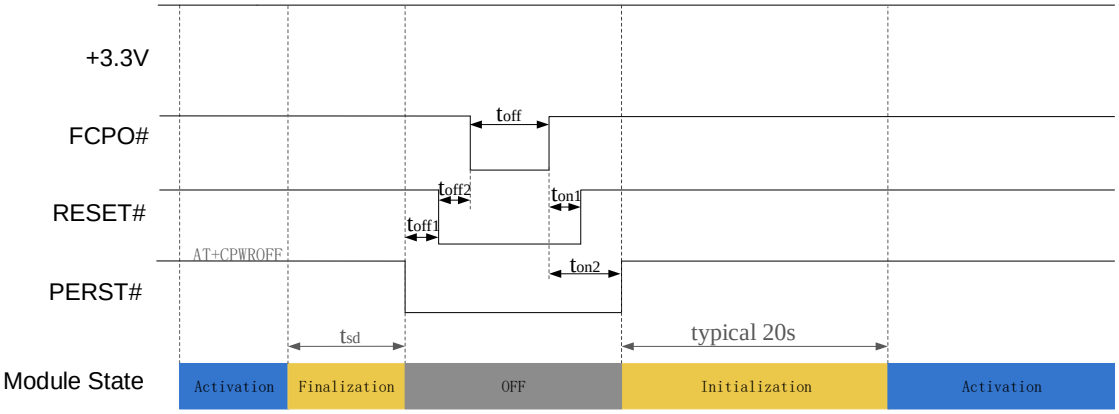

Figure 3-9 Reset control timing2nd

Index	Min.	Recommended	Max.	Comments
t_{off1}	16ms	20ms	-	RESET# should be asserted after PERST#, refer section 3.3.2
t_{off2}	2ms	10ms	-	FCPO# should be asserted after RESET#, refer section 3.3.2
t_{off}	500ms	500ms	-	Time to allow the WWAN module to fully discharge any residual voltages before the pin could be de-asserted again. This is required for both Pre-OS as well as Runtime flow

Index	Min.	Recommended	Max.	Comments
t_{on1}	20ms	20ms	-	RESET# should be de-asserted after FCPO#, refer section 3.3.1.2
t_{on2}	50ms	100ms	-	The time delay of PERST# de-asserted after FCPO#, PERST# must always be the last to get de-asserted, refer section 3.3.1.2

3.3.4 PCIe Link State

Modem has the lowest power consumption in D0 L1.2 PCIe link state, D3cold L2 will increase extra about TBD power consumption. CLKREQ# can assert or de-assert in D3cold L2, but CLKREQ# shouldn't be changed again during D3cold L2. When CLKREQ# asserts in D3cold L2, it will increase extra TBD power consumption compared with CLKREQ# de-asserted in D3cold L2, we recommend keep CLKREQ# de-asserted in D3cold L2.

PCIe Link State	PERST#	CLKREQ#	Power Consumption (mA)	Description
D0 L1.2	H	H	I_{sleep}	Refer 3.2.3 Power Consumption
$D3_{cold}$ L2	L	H	I_{sleep}+TBD	The extra TBD is consumed on PERST# pull down
	L	L	I_{sleep}+TBD	The extra TBD is consumed on CLKREQ# pull down

3.3.4.1 D0 L1.2

Module supports PCIe goes into D0 L1.2 state in Win10 OS. The D0 L0@S0/S0ix→ D0 L1.2@S0/S0ix→D0 L0@S0/S0ix timing is shown in figure 3-10:

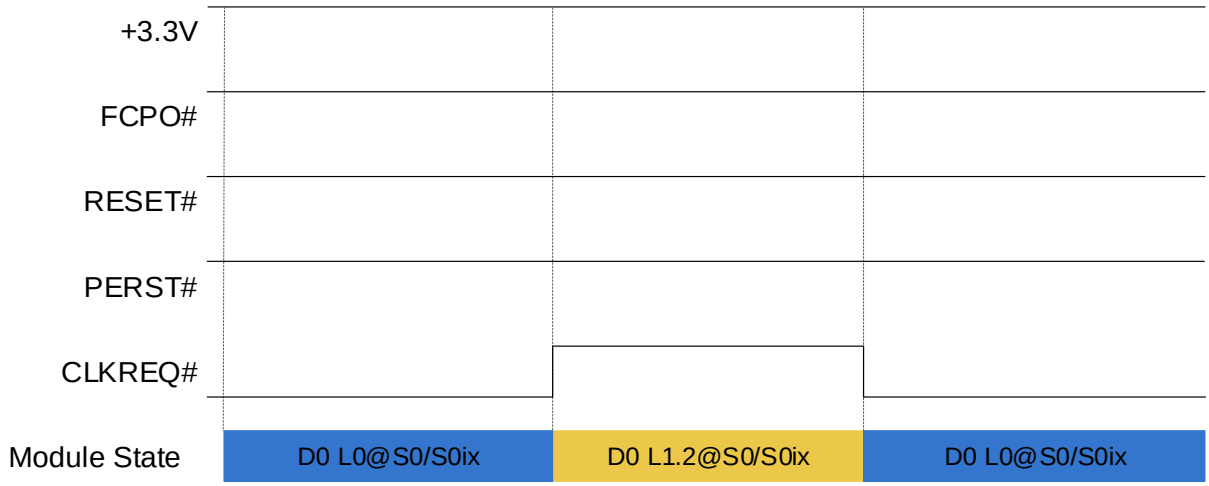

Figure 3-10 D0 L1.2 timing

3.3.4.2 D3cold L2

Module supports PCIe goes into D3cold L2 state in Win10 system. In D3cold L2 state, PCIe link can be wakeup by both modem and host. The D0 L0@S0/S0ix→D3cold L2@S0/S0ix→D0 L0@S0/S0ix timing is shown in Figure 3-11 and Figure 3-12:

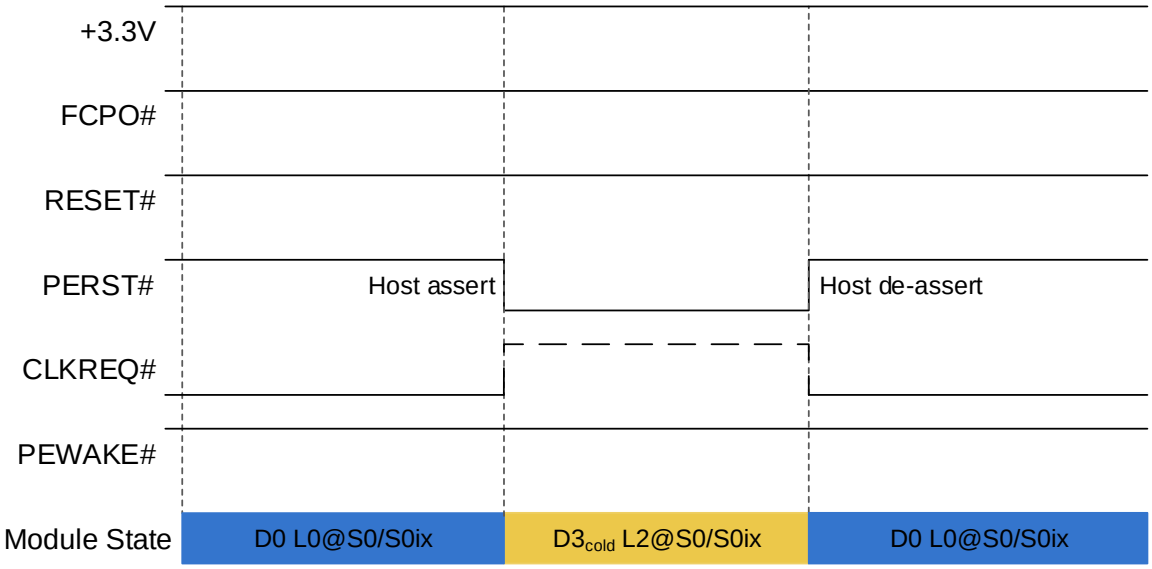

Figure 3-11 D3cold L2 timing (host wakeup)

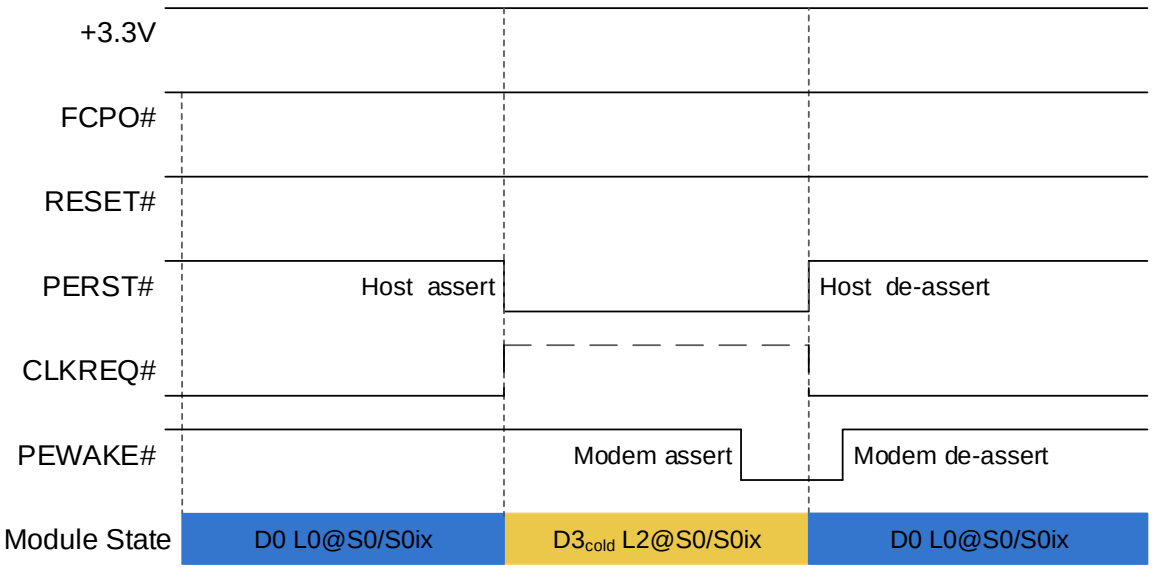

Figure 3-12 D3cold L2 timing (modem wakeup)

3.3.5 Timing Application

The recommended timing application in Win10 OS is as below table:

System status		Timing Application
S0ix (Modem standby)	D0 L1.2	Refer to section 3.3.4.1 Figure 3-10 D0 L1.2 Timing
	$D3_{cold}$ L2	Refer to section 3.3.4.2 Figure 3-11/3-12 $D3_{cold}$ L2 timing
S3, S4, S5	Power on (back to S0)	Refer to section 3.3.1.2 Figure 3-5 Timing control for start-up
	Power off (out of S0)	Refer to section 3.3.2 Figure 3-6 Software power off timing
G3 boot	Power on	Refer to section 3.3.1.2 Figure 3-5 Timing control for start-up
Warm boot		Refer to section 3.3.3 Figure 3-9 Reset timing 2nd
Modem FW upgrade / Modem recovery		Refer to section 3.3.3 Figure 3-8 Reset timing 1st

3.4 PCIe Interface

FM350 module supports PCIe as IPC interface for data transfer. The PCIe supports Gen3, one lane for data transmission channel, it is also compatible with PCIe Gen2 and Gen1. BIOS configuration must follow X86 platform BKC (Best Know Configuration) reference design.

PCIe interface initialized with host driver, then mapped MBIM & GNSS port in Win10 OS and RMNET & AT port in Chrome/Linux/Android OS. The MBIM and RMNET interfaces are used for data transfer, GNSS port is used for receiving GNSS data, AT port is used for AT command.

3.4.1 PCIe Interface Definition

PCIe interface is defined as below table:

Pin#	Pin Name	I/O	Reset Value	Description	Level
41	PETn0	O	-	PCIe TX Differential signals, negative	-
43	PETP0	O	-	PCIe TX Differential signals, positive	-
47	PERn0	I	-	PCIe RX Differential signals, negative	-
49	PERP0	I	-	PCIe RX Differential signals, positive	-
53	REFCLKN	I	-	PCIe Reference Clock signal Negative	-

Pin#	Pin Name	I/O	Reset Value	Description	Level
55	REFCLKP	I	-	PCIe Reference Clock signal Positive	-
50	PERST#	I	PU	Asserted to reset module PCIe interface default. If module went into coredump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ)	3.3/1.8V
52	CLKREQ#	I/O	PD	Asserted by device to request a PCIe reference clock be available (active clock state) in order to transmit data. It also used by L1 PM Sub states mechanism, asserted by either host or device to initiate an L1 exit. Active low, open drain output and should add external pull up on platform	3.3/1.8V
54	PEWAKE#	O	T	Asserted to wake up system and reactivate PCIe link from L2 to L0, it depends on system whether supports wake up functionality. Active low, open drain output and should add external pull up on platform	3.3/1.8V

3.4.2 PCIe Interface Application

The reference circuit is shown in Figure 3-13:

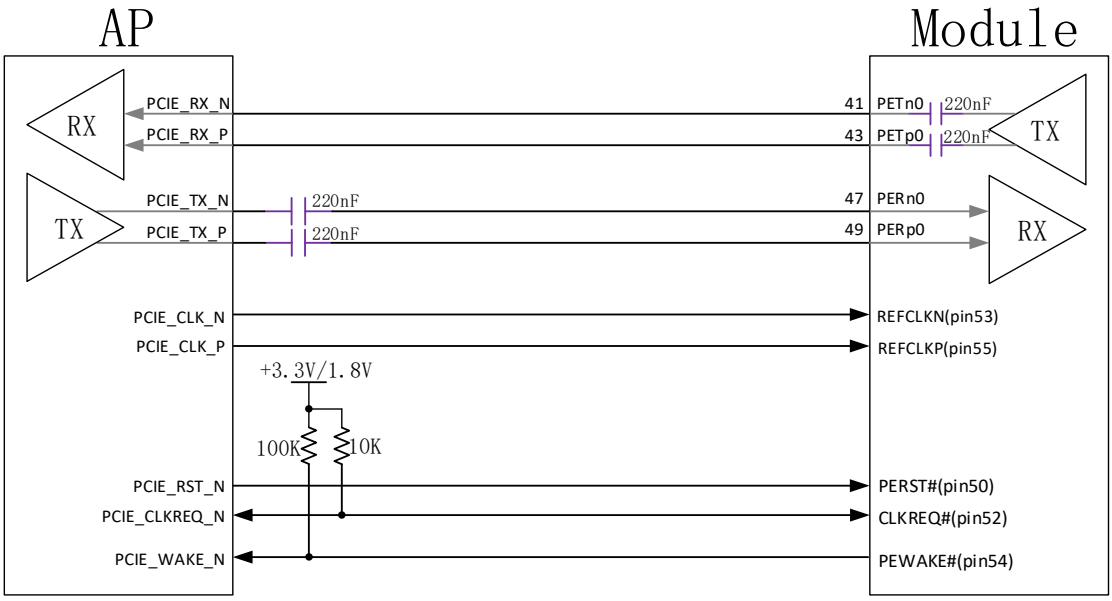

Figure 3-13 Reference Circuit for PCIe Interface

FM350 module supports PCIe Gen3/one lane, including three difference pairs: transmit pair TXP/N, receiving pair RXP/N and clock pair CLKP/N.

PCIe can achieve the maximum transmission rate of 8 GT/s, and must strictly follow the rules below in PCB Layout:

- The differential signal pair lines shall be parallel and equal in length;
- The differential signal pair lines shall be short if possible and be controlled within 7 inch (177.8 mm) for AP end;
- The impedance of differential pair lines is recommended to be 85Ω. All the impedance of differential pair should meet PCIe Gen3 protocol requirement of 70 to 100Ω;
- It shall avoid the discontinuous reference ground, such as segment and space;
- When the differential signal lines go through different layers, the via hole of grounding signal should be in close to that of signal, and generally, each pair of signals require 1-3 grounding signal via holes and the lines shall never cross the segment of plane;
- Try to avoid bended lines and avoid introducing common-mode noise in the system, which will influence the signal integrity and EMI of difference pair. As shown in Figure 3-14, the bending angle of all lines should be equal or greater than 135°, the spacing between difference pair lines should be larger than 20mil, and the line caused by bending should be greater than 1.5 times line width at least. When a serpentine line is used for length match with another line, the bended length of each segment shall be at least 3 times the line width (≥ 3W). The largest spacing between the bended part of the serpentine line and another one of the differential lines must be less than 2 times the spacing of normal differential lines (S1 < 2S);

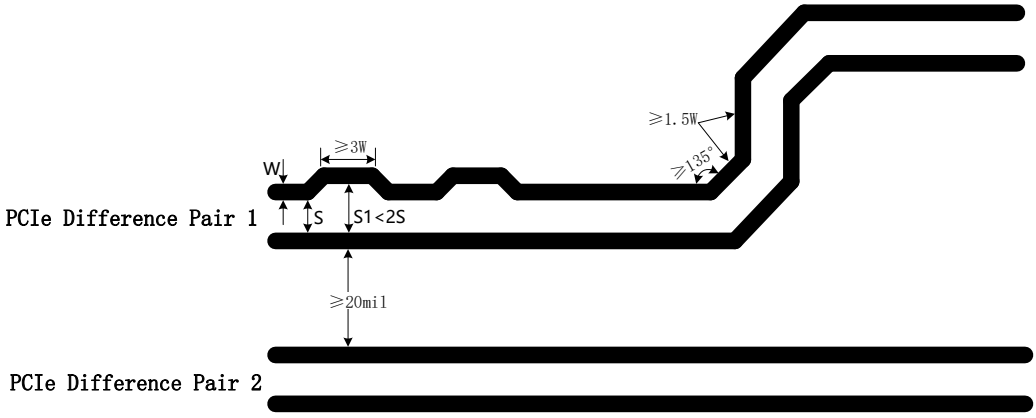

Figure 3-14 Requirement of PCIe line

- The difference in length of two data lines in difference pair should be within 5mil, and the length match is required for all parts. When the length match is conducted for the differential lines, the designed position of correct match should be close to that of incorrect match, as shown in Figure 3-15. However, there is no specific requirements for the length match of transmit pair and receiving pair, which means the length match is only required by intra differential pair rather than inter differential pair.

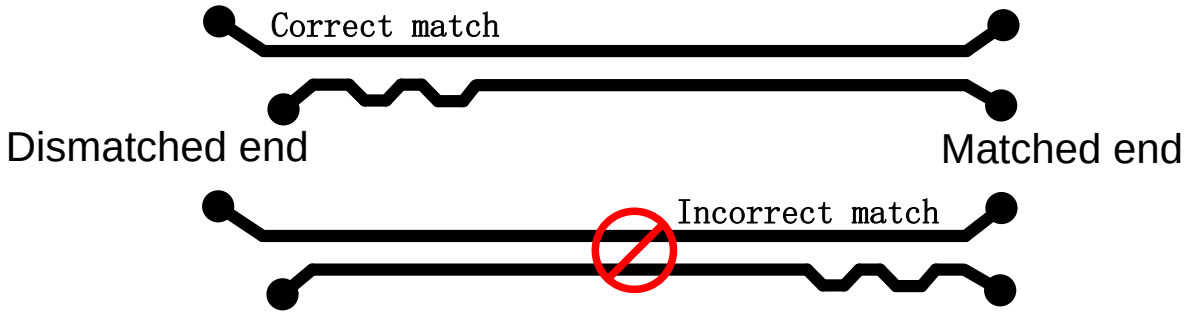

Figure 3-15 Length match design of PCIe difference pair

3.5 USIM Interface

The FM350 module supports dual SIM, one is a built-in eSIM and another is a SIM card interface. The SIM interface supports 1.8V and 3V SIM cards.

3.5.1 USIM Pins

The USIM1 pins description is shown in the following table:

Pin	Pin Name	I/O	Reset Value	Description	Level
36	UIM_PWR	PO	-	USIM power supply	1.8V/3V
30	UIM_RESET	O	PD	USIM reset	1.8V/3V
32	UIM_CLK	O	PD	USIM clock	1.8V/3V
34	UIM_DATA	I/O	PD	USIM data, internal pull up(4.7KΩ)	1.8V/3V
66	SIM_DETECT	I	PD	USIM card detect, internal 390K pull-up. Active high, and high level indicates SIM card is inserted; and low level indicates SIM card is detached.	1.8V

3.5.2 USIM Interface Circuit

3.5.2.1 N.C. SIM Card Slot

The reference circuit design for N.C. (Normally Closed) SIM card slot is shown in Figure 3-16:

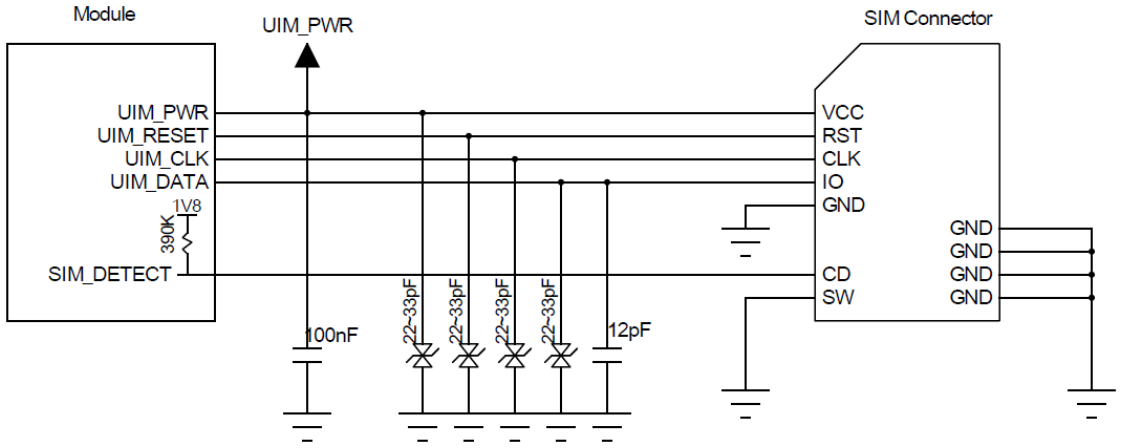

Figure 3-16 Reference circuit for N.C. SIM card slot

The principles of the N.C.SIM card slot are described as follows:

- When the SIM card is detached, it connects the short circuit between CD and SW pins, and drives the SIM_DETECT pin low.
- When the SIM card is inserted, it connects an open circuit between CD and SW pins, and drives the SIM_DETECT pin high.

3.5.2.2 N.O. SIM Card Slot

The reference circuit design for N.O. (Normally Open) SIM card slot is shown in Figure 3-17:

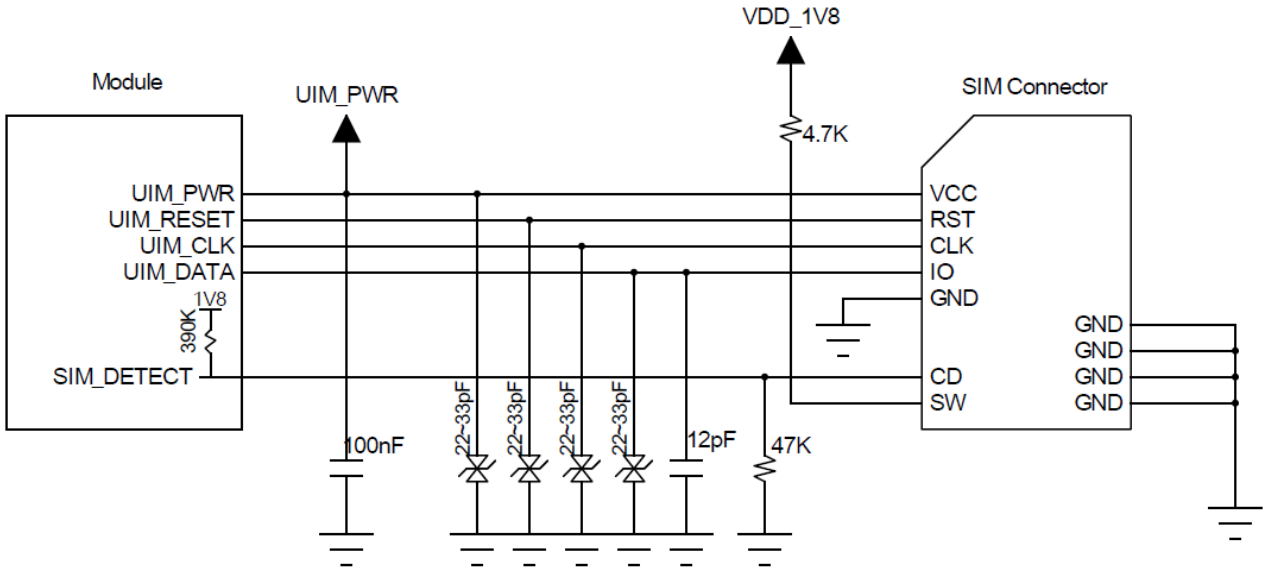

Figure 3-17 Reference circuit for N.O. SIM card slot

The principles of the N.O.SIM card slot are described as follows:

- When the SIM card is detached, it connects an open circuit between CD and SW pins, and drives the SIM_DETECT pin low.
- When the SIM card is inserted, it connects the short circuit between CD and SW pins, and drives the SIM_DETECT pin high.

3.5.3 USIM Hot-plug

The FM350 module supports the SIM card hot-plugging function, which determines whether the SIM card is inserted or detached by detecting the SIM_DETECT pin state of the SIM card slot.

The SIM card hot-plugging function can be configured by “AT+MSMPD” command, and the description for AT command is shown in the following table:

AT Command	Hot-plug Detection	Function Description
AT+MSMPD=1	Enable	Default value, the SIM card hot-plugging detection function is enabled. The module can detect whether the SIM card is inserted or not through the SIM_DETECT pin state.
AT+MSMPD=0	Disable	The SIM card hot-plugging detect function is disabled. The module reads the SIM card when starting up, and the SIM_DETECT status will not be detected.

Note:

SIM_DETECT is active high, it can be swapped to active low by AT CMD.

3.5.4 USIM Design

The SIM card circuit design should meet the EMC standards and ESD requirements with the improved capability to resist interference, to ensure that the SIM card can work stably. The following guidelines should be noted in design:

- The SIM card slot should be placed as close as possible to the module, and away from the RF antenna, DC/DC power supply, clock signal lines, and other strong interference sources.
- The SIM card slot with a metal shielding housing can improve the anti-interference ability.
- In order to make sure the SIM work stably, the SIM signal quality MUST meet SIM standards “*ETSI TS 102.221 Physical and logical characteristics*”. If the trace length of the SIM card signal is controlled less than 100mm, it will be easier to meet to the SIM signal specification.
- The trace length between the SIM card slot and the module should not exceed 100mm, or it could reduce the signal quality.
- The UIM_CLK and UIM_DATA signal lines should be isolated by GND to avoid crosstalk interference. If it is difficult for the layout, the whole SIM signal lines should be wrapped with GND as a group at least.
- The filter capacitors and ESD devices for SIM card signals should be placed near to the SIM card slot, and the ESD devices with 22 to 33pF capacitance should be used.

3.6 Status Indicator

The FM350 module provides two signals to indicate the operating status of the module, and the status indicator pins is shown in the following table:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
10	LED1#	O	T	System status LED, drain output.	3.3V
23	WOWWAN#	O	PD	Wake up host, Reserved	1.8V

3.6.1 LED#1 Signal

The LED#1 signal is used to indicate the operating status of the module, and the detailed description is shown in the following table:

Module Status	LED1# Signal
RF function ON	Low level (LED On)
RF function OFF	High level (LED Off)

The LED driving circuit is shown in figure 3-18:

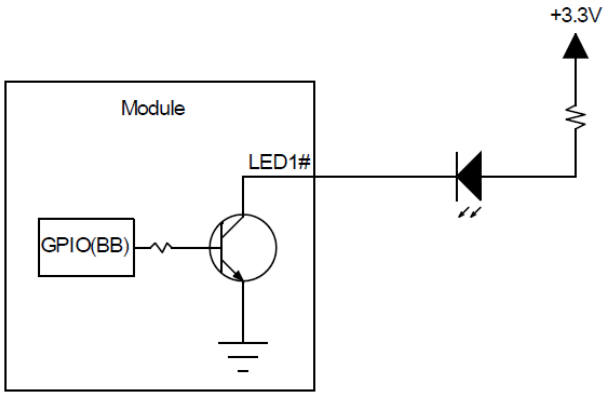

Figure 3-18 LED driving circuit

Note:

The resistance of LED current-limiting resistor is selected according to the driving voltage and the driving current.

3.6.2 WOWWAN#

The WOWWAN# signal is used to wake the Host (AP) when there comes the data request. The definition of WOWWAN# signal is as follows:

Operating Mode	WOWWAN# Signal
SMS or data requests	Pull low 1s then pull high (pulse signal).
Idle/Sleep	High level

The WOWWAN# timing is shown in Figure 3-19:

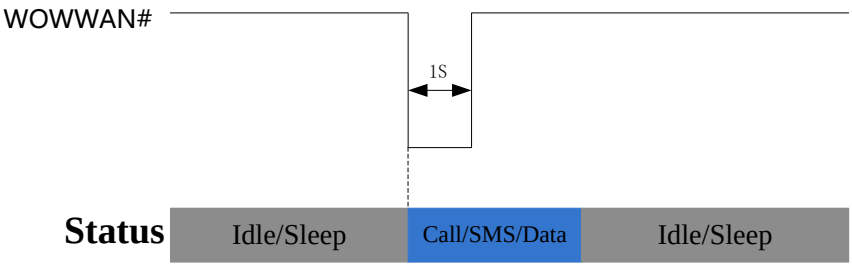

Figure 3-19 WOWWAN# timing

Note:
WOWWAN# is disabled in default, it can be enabled by AT CMD: AT+GTWAKE=1 and restart module.

3.7 Interrupt Control

The FM350 module provides four interrupt signals, and the pin definition is as follows:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
8	W_DISABLE1#	I	PD	Enable/Disable RF network	3.3/1.8V
25	DPR	I	PD	Dynamic Power Reduction - Body SAR control signal (SAR_BACK_OFF)	3.3/1.8V
26	W_DISABLE2#	I	PD	GNSS Disable signal Reserved	3.3/1.8V

3.7.1 W_DISABLE1#

The module provides a hardware pin to enable/disable WWAN RF function, and the function can also be controlled by the AT command. The module enters the flight mode after the RF function is disabled. The definition of W_DISABLE1# signal is as below table:

W_DISABLE1# signal	Function
High/Floating	WWAN function is enabled, the module exits the flight mode.
Low	WWAN function is disabled, the module enters flight mode.

Note：

The function of W_DISABLE1# is disabled in default, it can be enabled by AT CMD: AT+GTFMODE=1 and restart module.

3.7.2 BODYSAR

The FM350 module supports Body SAR function by detecting the DPR pin. The voltage level of DPR is high by default, and when the SAR sensor detects the closing human body, the DPR signal will be pulled down. As the result, the module then lowers down its emission power to its default threshold value, thus reducing the RF radiation on the human body. The threshold of emission power can be set by the AT Commands. The definition of DPR signal is shown in the following table:

DPR signal	Function
High/Floating	The module keeps the default emission power
Low	Lower the maximum emission power to the threshold value of the module.

3.8 ANT Tunable Interface

The module supports ANT Tunable interfaces with two different control modes, i.e. MIPI interface and 4bit GPO interface. Through cooperating with external antenna adapter switch via ANT tunable, it can flexibly configure the bands of LTE antenna to improve the antenna's working efficiency and save space for the antenna. Module also support 1.8V output for antenna tuner. The pin definition is as below table:

Pin	Pin Name	I/O	Pin Description	Level
24	ANT_TUNER_1V8	O	1.8V power output for antenna tuner, can mux as GPIO. Reserved	1.8V
56	RFFE_SCLK	O	Tunable ANT control, MIPI Interface, RFFE clock	1.8V
58	RFFE_SDATA	I/O	Tunable ANT control, MIPI Interface, RFFE data	1.8V

Pin	Pin Name	I/O	Pin Description	Level
59	ANTCTL0	O	Tunable ANT control, GPO interface, Bit0	1.8V
61	ANTCTL1	O	Tunable ANT control, GPO interface, bit1	1.8V
63	ANTCTL2	O	Tunable ANT control, GPO interface, Bit2	1.8V
65	ANTCTL3	O	Tunable ANT control, GPO interface, Bit3	1.8V

3.9 Configuration Interface

The FM350 module provides four pins for the configuration as the WWAN-PCIe, type M.2 module:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
1	CONFIG_3	O	-	NC	-
21	CONFIG_0	O	-	NC	-
69	CONFIG_1	O	L	Internally connected to GND	-
75	CONFIG_2	O	-	NC	-

The M.2 module configuration is the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	WWAN–PCIe Gen3, USB3.1 Gen1	Vendor defined

Please refer to *"PCI Express M.2 Specification Rev1.2"* for more details.

4 Radio Frequency

4.1 RF Interface

4.1.1 RF Interface Functionality

The FM350 module supports four RF connectors used for external antenna connection. As the Figure 4-1 shows, “M” is for Main antenna, used to receive and transmit RF signals, “D/G” is for Diversity antenna, used to receive the diversity RF signals. “M1” and “M2” are used for supporting 4x4 MIMO data transfer.

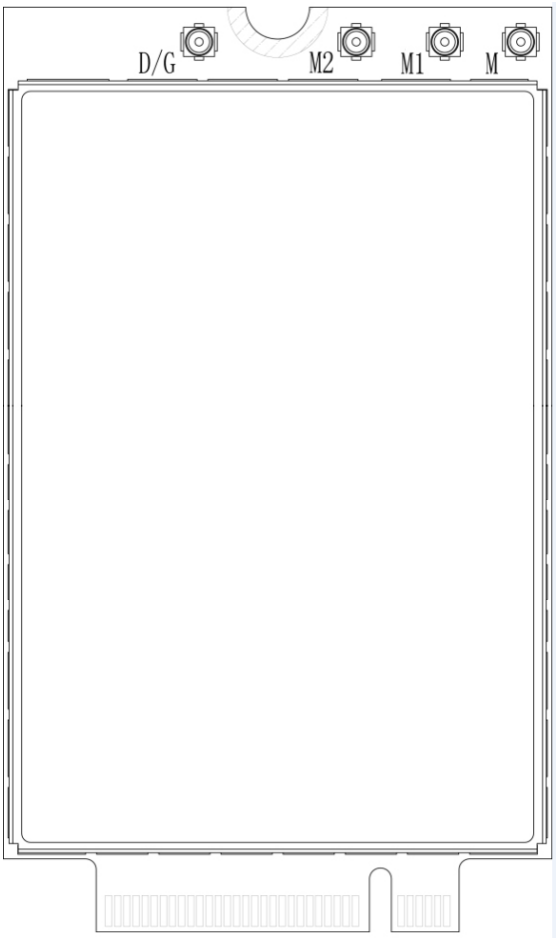

Figure 4-1 RF connectors

4.1.2 RF Connector Characteristic

Rated Condition		Environment Condition
Frequency Range	DC~6GHz	Temperature Range: –40°C to +85°C
Characteristic Impedance	50Ω	

4.1.3 RF Connector Dimension

FM350 module uses standard M.2 RF connectors. The RF connector part number is 818004607 manufactured by ECT Corporation, and the connector size is 2x2x0.6m. The connector dimension is shown as following picture:

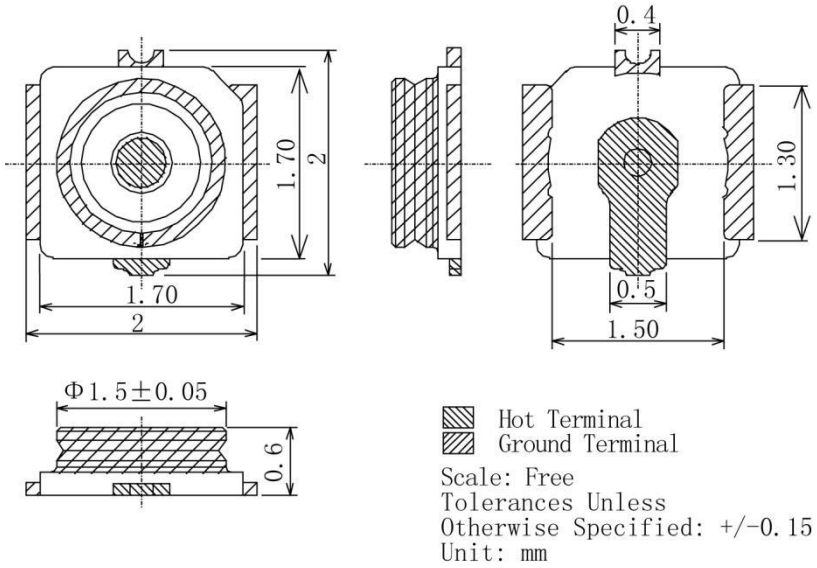

Figure 4-2 RF connector dimensions

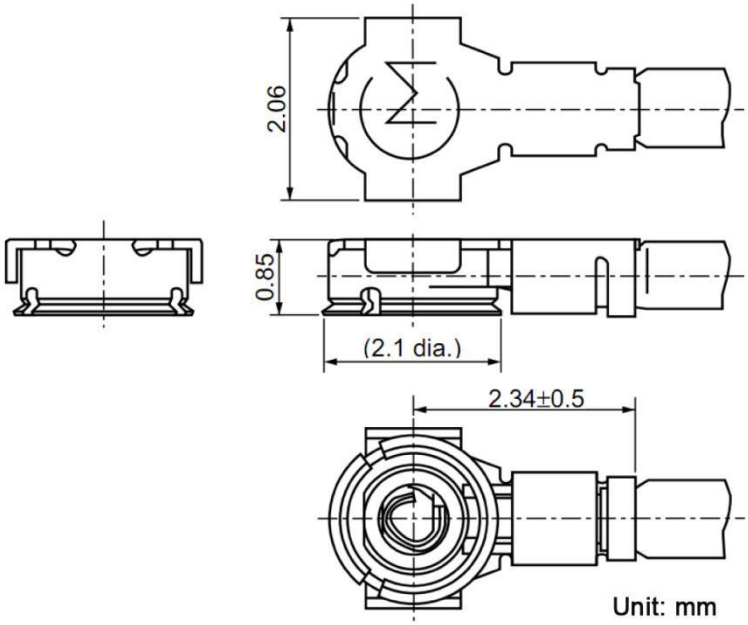

Figure 4-3 0.81mm coaxial antenna dimensions

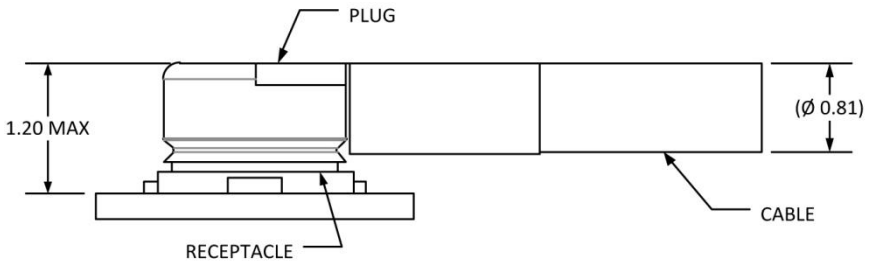

Figure 4-4 Schematic diagram of 0.81mm coaxial antenna connected to the RF connector

4.1.4 RF Connector Assembly

Mate RF connector parallel refer Figure 4-5, do not slant mate with strong force.

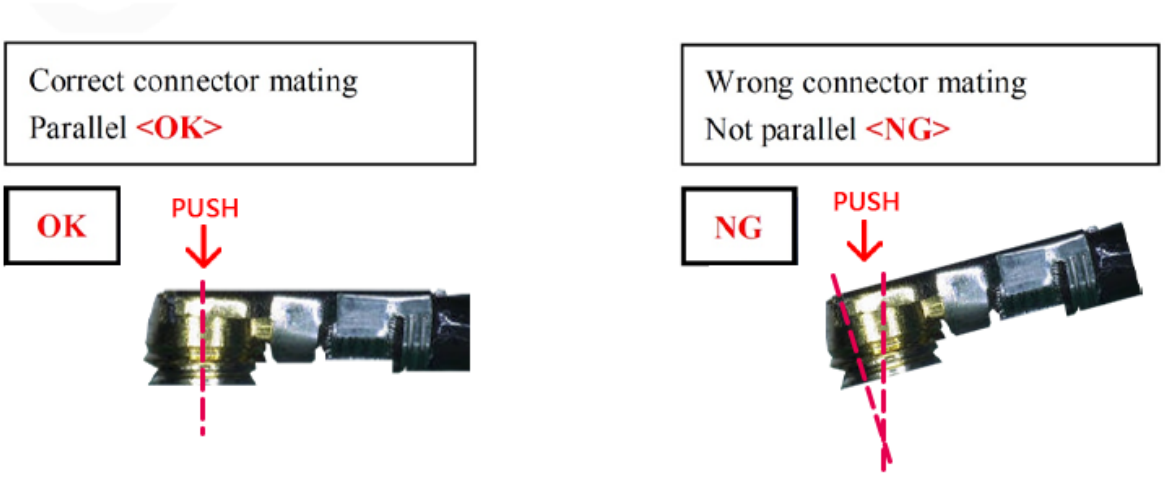

Figure 4-5 Mate RF connector

To avoid damage in RF connector unmating, it is recommended using pulling JIG as Figure 4-6, and the pulling JIG must be lifted up vertically to PCB surface (see Figure 4-7 and 4-8).

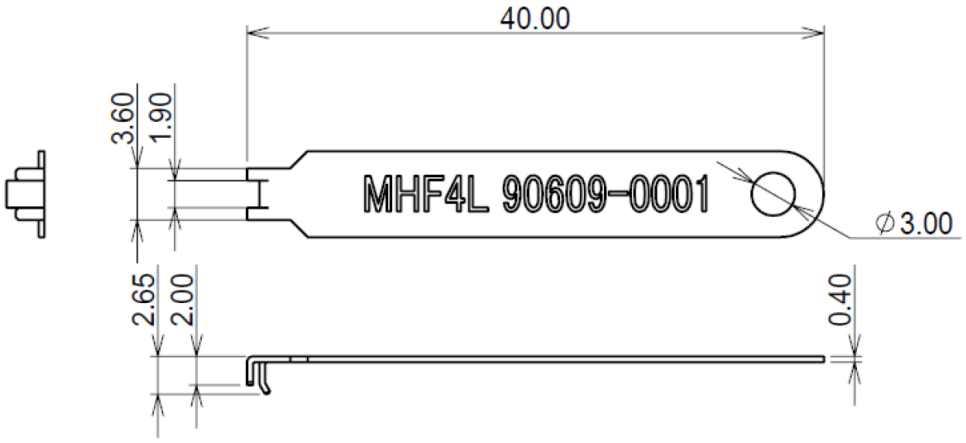

Figure 4-6 Pulling JIG

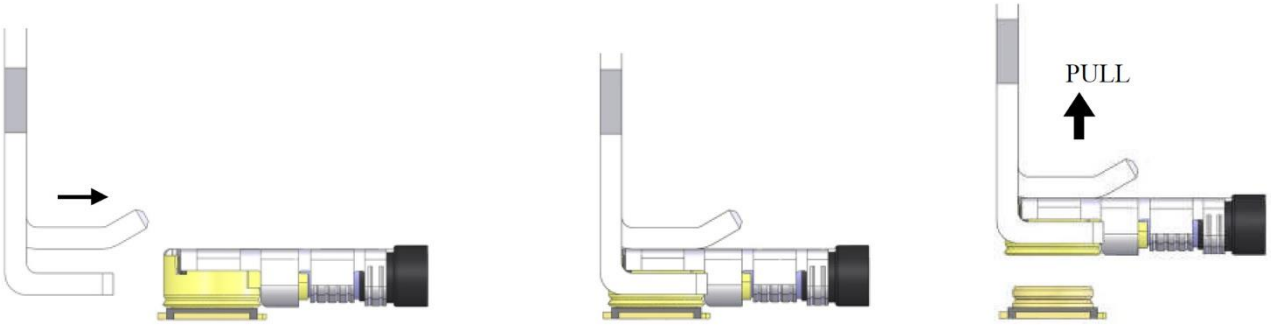

Figure 4-7 Lift up pulling JIG

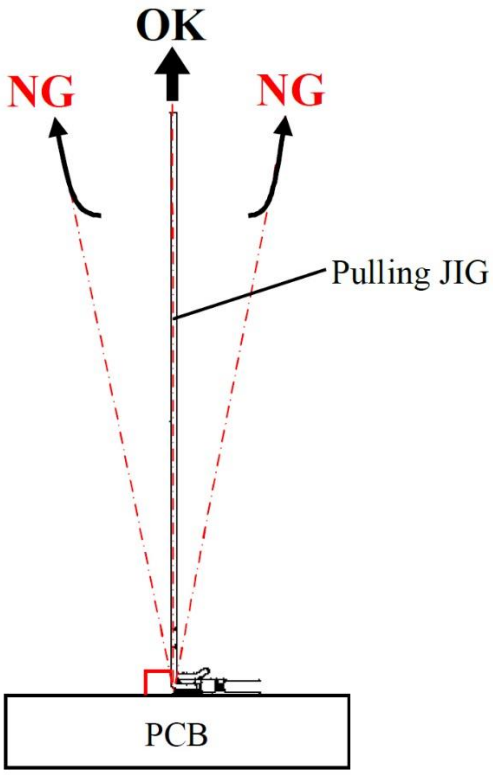

Figure 4-8 Pulling direction

4.2 Operating Band

The FM350 module operating bands of the antennas are shown in the following table:

Operating Band	Description	RAT	TX (MHz)	RX (MHz)
Band 1	2100MHz	LTE FDD/WCDMA	1920 - 1980	2110 - 2170
Band 2	1900MHz	LTE FDD/WCDMA	1850 - 1910	1930 - 1990
Band 3	1800MHz	LTE FDD	1710 - 1785	1805 - 1880
Band 4	1700MHz	LTE FDD/WCDMA	1710 - 1755	2110 - 2155
Band 5	850MHz	LTE FDD/WCDMA	824 - 849	869 - 894
Band 7	2600Mhz	LTE FDD	2500 - 2570	2620 - 2690
Band 8	900MHz	LTE FDD/WCDMA	880 - 915	925 - 960
Band 12	700MHz	LTE FDD	699 - 716	729 - 746
Band 13	700MHz	LTE FDD	777 - 787	746 - 756
Band 14	700MHz	LTE FDD	788 - 798	758 - 768
Band 17	700MHz	LTE FDD	704 - 716	734 - 746
Band 18	800MHz	LTE FDD	815 - 830	860 - 875
Band 19	850MHz	LTE FDD	830 - 845	875 - 890
Band 20	800MHz	LTE FDD	832 - 862	791 - 821
Band 25	1900MHz	LTE FDD	1850 - 1915	1930 - 1995
Band 26	850MHz	LTE FDD	814 - 849	859 - 894
Band 28	700MHz	LTE FDD	703 - 748	758 - 803
Band 29	700MHz	LTE FDD	-	717 - 728
Band 30	2300MHz	LTE FDD	2305 - 2315	2350 - 2360
Band 32	1500MHz	LTE FDD	-	1452 - 1496
Band 34	2000MHz	LTE TDD	2010 -2025	
Band 38	2600MHz	LTE TDD	2570 - 2620	
Band 39	1900MHZ	LTE TDD	1880 - 1920	
Band 40	2300MHz	LTE TDD	2300 - 2400	
Band 41	2500MHz	LTE TDD	2496 - 2690	
Band 42	3500MHZ	LTE TDD	3400 - 3600	

Operating Band	Description	RAT	TX (MHz)	RX (MHz)
Band 43	3700MHz	LTE TDD	3600 - 3800	
Band 46	5200MHZ	LTE TDD	-	5150 - 5925
Band 48	3600MHz	LTE TDD	3550 – 3700	
Band 66	1700MHz	LTE FDD	1710 - 1780	2110 - 2200
Band 71	600MHz	LTE FDD	663 -698	617 - 652
n1	2100MHz	NR FDD	1920 - 1980	2110 - 2170
n2	1900MHz	NR FDD	1850 - 1910	1930 - 1990
n3	1800MHz	NR FDD	1710 - 1785	1805 - 1880
n5	850MHz	NR FDD	824 - 849	869 - 894
n7	2600Mhz	NR FDD	2500 - 2570	2620 - 2690
n8	900MHz	NR FDD	880 - 915	925 - 960
n20	800MHz	NR FDD	832 - 862	791 - 821
n25	1900MHz	NR FDD	1850 - 1915	1930 - 1995
n28	700MHz	NR FDD	703 - 748	758 - 803
n30	2300MHz	NR FDD	2305 - 2315	2350 - 2360
n38	2600MHz	NR TDD	2570 - 2620	
n40	2300MHz	NR TDD	2300 - 2400	
n41	2500MHz	NR TDD	2496 - 2690	
n48	3500MHz	NR TDD	3550 - 3700	
n66	1700MHz	NR FDD	1710 - 1780	2110 - 2200
n71	600MHz	NR FDD	663 - 698	617 - 652
n77		NR TDD	3300 - 4200	
n78		NR TDD	3300 - 3800	
n79		NR TDD	4400 - 5000	
GPS L1	-	-	-	1575.42±1.023
GLONASS G1	-	-	-	1602.5625±4
Galileo E1	-	-	-	1575.42±2.046
BDS B1	-	-	-	1561.098±2.046

4.3 Transmitting Power

The transmitting power for each band of the FM350 module is shown in the following table:

RAT	Band	3GPP Requirement (dBm)	Tx Power (dBm)	Note
WCDMA	Band 1	24+1.7/-3.7	23.5±1	-
	Band 2	24+1.7/-3.7	23.5±1	-
	Band 4	24+1.7/-3.7	23.5±1	-
	Band 5	24+1.7/-3.7	23.5+2/-1	-
	Band 8	24+1.7/-3.7	23.5+2/-1	-
LTE	Band 1	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 2	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 3	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 4	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 5	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 7	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 8	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 12	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 13	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 14	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 17	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 18	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 19	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 20	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 25	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 26	23±2.7	23+2/-1	10MHz Bandwidth, 1 RB
	Band 28	23+2.7/-3.2	23+2/-1	10MHz Bandwidth, 1 RB
	Band 30	23±2.7	22±1	10MHz Bandwidth, 1 RB
	Band 34	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 38	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 39	23±2.7	23±1	10MHz Bandwidth, 1 RB

RAT	Band	3GPP Requirement (dBm)	Tx Power (dBm)	Note
	Band 40	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 41	26±2.7	26±1	10MHz Bandwidth, 1 RB
	Band 42	23+3/-4	23±1	10MHz Bandwidth, 1 RB
	Band 43	23+3/-4	23±1	10MHz Bandwidth, 1 RB
	Band 48	23+3/-4	21±1	10MHz Bandwidth, 1 RB
	Band 66	23±2.7	23±1	10MHz Bandwidth, 1 RB
	Band 71	23+2.7/-3.2	23+2/-1	10MHz Bandwidth, 1 RB
NR	n1	23±2.7	23±1	15MHz BW, Inner RB
	n2	23±2.7	23±1	15MHz BW, Inner RB
	n3	23±2.7	23±1	20MHz BW, Inner RB
	n5	23±2.7	23+2/-1	15MHz BW, Inner RB
	n7	23±2.7	23±1	15MHz BW, Inner RB
	n8	23±2.7	23+2/-1	15MHz BW, Inner RB
	n20	23±2.7	23+2/-1	15MHz BW, Inner RB
	n25	23±2.7	23±1	15MHz BW, Inner RB
	n28	23+2.7/-3.2	23+2/-1	15MHz BW, Inner RB
	n30	23±2.7	22±1	10MHz BW, Inner RB
	n38	23±2.7	23±1	15MHz BW, Inner RB
	n40	23±2.7	23±1	15MHz BW, Inner RB
	n41	26+2.7/-3.7	26±1	60MHz BW, Inner RB
	n48	23+3/-4	21±1	20MHz BW, Inner RB
	n66	23±2.7	23±1	20MHz BW, Inner RB
	n71	23+2.7/-3.2	23+2/-1	10MHz BW, Inner RB
	n77	26+3/-4	25±1	50MHz BW, Inner RB
	n78	26+3/-4	26±1	50MHz BW, Inner RB
	n79	26+3/-4	26±1	60MHz BW, Inner RB

4.4 Receiver Sensitivity

4.4.1 Dual Antenna Receiver Sensitivity

All bands support dual antenna, the receiver sensitivity for each band of FM350 module is shown in the following table:

RAT	Band	3GPP Requirement (dBm)	RX Sensitivity Typical (dBm)	Note
WCDMA	Band 1	-106.7	TBD	-
	Band 2	-104.7	TBD	-
	Band 4	-106.7	TBD	-
	Band 5	-104.7	TBD	-
	Band 8	-103.7	TBD	-
LTE FDD	Band 1	-96.3	TBD	10MHz Bandwidth
	Band 2	-94.3	TBD	10MHz Bandwidth
	Band 3	-93.3	TBD	10MHz Bandwidth
	Band 4	-96.3	TBD	10MHz Bandwidth
	Band 5	-94.3	TBD	10MHz Bandwidth
	Band 7	-94.3	TBD	10MHz Bandwidth
	Band 8	-93.3	TBD	10MHz Bandwidth
	Band 12	-93.3	TBD	10MHz Bandwidth
	Band 13	-93.3	TBD	10MHz Bandwidth
	Band 14	-93.3	TBD	10MHz Bandwidth
	Band 17	-93.3	TBD	10MHz Bandwidth
	Band 18	-96.3	TBD	10MHz Bandwidth
	Band 19	-96.3	TBD	10MHz Bandwidth
	Band 20	-93.3	TBD	10MHz Bandwidth
	Band 25	-92.8	TBD	10MHz Bandwidth
	Band 26	-93.8	TBD	10MHz Bandwidth
	Band 28	-94.8	TBD	10MHz Bandwidth
	Band 29	-93.3	TBD	10MHz Bandwidth
	Band 30	-95.3	TBD	10MHz Bandwidth

RAT	Band	3GPP Requirement (dBm)	RX Sensitivity Typical (dBm)	Note
	Band 32	-96.3	TBD	10MHz Bandwidth
	Band 46	-88.5	TBD	20MHz Bandwidth
	Band 66	-95.8	TBD	10MHz Bandwidth
	Band 71	-93.5	TBD	10MHz Bandwidth
LTE TDD	Band 34	-96.3	TBD	10MHz Bandwidth
	Band 38	-96.3	TBD	10MHz Bandwidth
	Band 39	-96.3	TBD	10MHz Bandwidth
	Band 40	-96.3	TBD	10MHz Bandwidth
	Band 41	-94.3	TBD	10MHz Bandwidth
	Band 42	-95	TBD	10MHz Bandwidth
	Band 43	-95	TBD	10MHz Bandwidth
	Band 48	-95	TBD	10MHz Bandwidth
NR	n1	-94.3	TBD	SCS 15KHz 15MHz BW
	n2	-92.3	TBD	SCS 15KHz 15MHz BW
	n3	-90.1	TBD	SCS 15KHz 20MHz BW
	n5	-92.3	TBD	SCS 15KHz 15MHz BW
	n7	-92.3	TBD	SCS 15KHz 15MHz BW
	n8	-91.3	TBD	SCS 15KHz 15MHz BW
	n20	-90.3	TBD	SCS 15KHz 15MHz BW
	n25	-90.8	TBD	SCS 15KHz 15MHz BW
	n28	-92.8	TBD	SCS 15KHz 15MHz BW
	n30	-95.1	TBD	SCS 15KHz 10MHz BW
	n38	-94.4	TBD	SCS 30KHz 15MHz BW
	n40	-91.3	TBD	SCS 30KHz 30MHz BW
	n41	-86.2	TBD	SCS 30KHz 60MHz BW
	n48	-91.9	TBD	SCS 30KHz 20MHz BW
	n66	-92.6	TBD	SCS 15KHz 20MHz BW
	n71	-90.9	TBD	SCS 15KHz 10MHz BW

RAT	Band	3GPP Requirement (dBm)	RX Sensitivity Typical (dBm)	Note
	n77	-87.2	TBD	SCS 30KHz 50MHz BW
	n78	-87.7	TBD	SCS 30KHz 50MHz BW
	n79	-86.9	TBD	SCS 30KHz 60MHz BW

Note:

1. The above values are measured in dual antennas condition (Main+Diversity). For single main antenna (without Diversity), the sensitivity will drop around 3dBm for each band.
2. B29 dual antenna receiver sensitivity test is at DL CA: CA_2A-29A
3. B32 dual antenna receiver sensitivity test is at DL CA: CA_20A-32A
4. B46 dual antenna receiver sensitivity test is at DL CA: CA_13A-46A

4.4.2 Four Antenna Receiver Sensitivity

Some bands support four antennas, the receiver sensitivity for some bands of FM350 module is shown in below table:

Mode	Band	3GPP Requirement (dBm)	RX Sensitivity Typical (dBm)	Note
LTE FDD	Band 1	-99	TBD	10MHz Bandwidth
	Band 2	-97	TBD	10MHz Bandwidth
	Band 3	-96	TBD	10MHz Bandwidth
	Band 4	-99	TBD	10MHz Bandwidth
	Band 7	-97	TBD	10MHz Bandwidth
	Band 25	-95.5	TBD	10MHz Bandwidth
	Band 30	-98	TBD	10MHz Bandwidth
	Band 66	-98.5	TBD	10MHz Bandwidth
LTE TDD	Band 34	-99	TBD	10MHz Bandwidth
	Band 38	-99	TBD	10MHz Bandwidth
	Band 39	-99	TBD	10MHz Bandwidth
	Band 40	-99	TBD	10MHz Bandwidth
	Band 41	-97	TBD	10MHz Bandwidth
	Band 42	-97.2	TBD	10MHz Bandwidth
	Band 43	-97.2	TBD	10MHz Bandwidth

Mode	Band	3GPP Requirement (dBm)	RX Sensitivity Typical (dBm)	Note
	Band 48	-97.2	TBD	10MHz Bandwidth
NR	n1	-97	TBD	SCS 15KHz 15MHz BW
	n2	-95	TBD	SCS 15KHz 15MHz BW
	n3	-92.8	TBD	SCS 15KHz 20MHz BW
	n7	-95	TBD	SCS 15KHz 15MHz BW
	n25	-93.5	TBD	SCS 15KHz 15MHz BW
	n30	-97.8	TBD	SCS 15KHz 10MHz BW
	n38	-97.1	TBD	SCS 30KHz 15MHz BW
	n40	-94	TBD	SCS 30KHz 30MHz BW
	n41	-88.9	TBD	SCS 30KHz 60MHz BW
	n48	-94.1	TBD	SCS 30KHz 20MHz BW
	n66	-95.3	TBD	SCS 15KHz 20MHz BW
	n77	-89.4	TBD	SCS 30KHz 50MHz BW
	n78	-89.9	TBD	SCS 30KHz 50MHz BW
	n79	-89.1	TBD	SCS 30KHz 60MHz BW

Note:

The above values are measured in four antennas condition (Main+Diversity+M1+M2). If only use dual antennas (Main+Diversity), the sensitivity will drop about 3dBm for each band.

4.5 GNSS

FM350 module supports GNSS with D/G antenna, the GNSS includes GPS/GLONASS/ Galileo/BDS/QZSS. GNSS feature and performance are as below table:

Description	Condition	Test Result	
		Max	Typical
Current	Fixing	TBD	TBD
	Tracking	TBD	TBD
	Sleep	TBD	TBD
TTFF	Cold start	TBD	TBD
	Warm start	TBD	TBD
	Hot Start	TBD	TBD
Sensitivity	Tracking	TBD	TBD
	Acquisition	TBD	TBD

Note:

GNSS current is tested with RF disabled at 25℃ temperature.

4.6 Antenna Design

The FM350 module provides four antenna interfaces, and the antenna design requirements is shown in the following table:

FM350 Module Main Antenna Requirement	
Frequency range	The most proper antenna to adapt the frequencies should be used.
Bandwidth(WCDMA)	WCDMA band 1 (2100): 250MHz WCDMA band 2 (1900): 140MHz WCDMA band 4 (1700): 445MHz WCDMA band 5 (850): 70MHz WCDMA band 8 (900): 80MHz
Bandwidth(LTE)	LTE band 1 (2100): 250MHz LTE band 2 (1900): 140MHz LTE Band 3 (1800): 170MHz LTE band 4 (1700): 445MHz LTE band 5 (850): 70MHz LTE band 7 (2600): 190MHz LTE Band 8 (900): 80MHz LTE band 12 (700): 47MHz LTE band 13 (700): 41MHz LTE band 14 (700): 40MHz LTE band 17 (700): 42MHz LTE band 18 (800): 80MHz LTE band 19 (850): 80MHz LTE band 20 (800): 71MHz LTE band 25 (1900): 145MHz LTE band 26 (850): 80MHz LTE band 28 (700): 100MHz LTE band 29 (700): 11MHz LTE band 30 (2300): 55MHz LTE band 32 (1500): 44MHz LTE band 34 (2000): 15MHz LTE band 38 (2600): 50MHz LTE band 39 (1900): 40MHz LTE band 40 (2300): 100MHz LTE band 41 (2500): 110MHz LTE band 42 (3500): 200MHz LTE band 43 (3700): 200MHz LTE band 46 (5500): 775MHz LTE band 48 (3600): 150MHz LTE band 66 (1700): 490MHz LTE band 71 (600): 81MHz
NR	n1 (2100): 250MHz n2 (1900): 140MHz n3 (1800): 170MHz

FM350 Module Main Antenna Requirement	
	n5 (850): 70MHz n7 (2600): 190MHz n8 (900): 80MHz n20 (800): 71MHz n25 (1900): 145MHz n30 (2300): 55MHz n28 (700): 100MHz n38 (2600): 50MHz n40 (2300): 100MHz n41 (2500): 110MHz n66 (1700): 490MHz n71 (600): 35MHz n77 (3750): 900MHz n78 (3500): 500MHz n79 (5500): 600MHz
Bandwidth(GNSS)	GPS: 2MHz GLONASS: 8MHz Galileo: 8MHz BDS: 4MHz QZSS: TBD
Impedance	50Ω
Input power	> 28dBm average power WCDMA & LTE & NR
Recommended standing-wave ratio (SWR)	≤ 2:1

5 ESD Characteristics

The module is generally not protected against Electrostatic Discharge (ESD). ESD handling precautions that apply to ESD sensitive components should be strictly followed. Proper ESD handling procedures must be applied throughout the processing, handling, assembly and operation of any application with module. The ESD characteristics are shown in the following table (Temperature: 25°C, Relative Humidity: 40%).

Interface	Contact Discharge	Air Discharge
GND	±8 kV	±15 kV
Antenna Interface	±8 kV	NA
Golden Finger	±2 kV	NA

Note：

ESD performance is based on EVB-M2 development board.

6 Structure Specification

6.1 Product Appearance

The product appearance for FM350 module is shown in Figure 6-1:

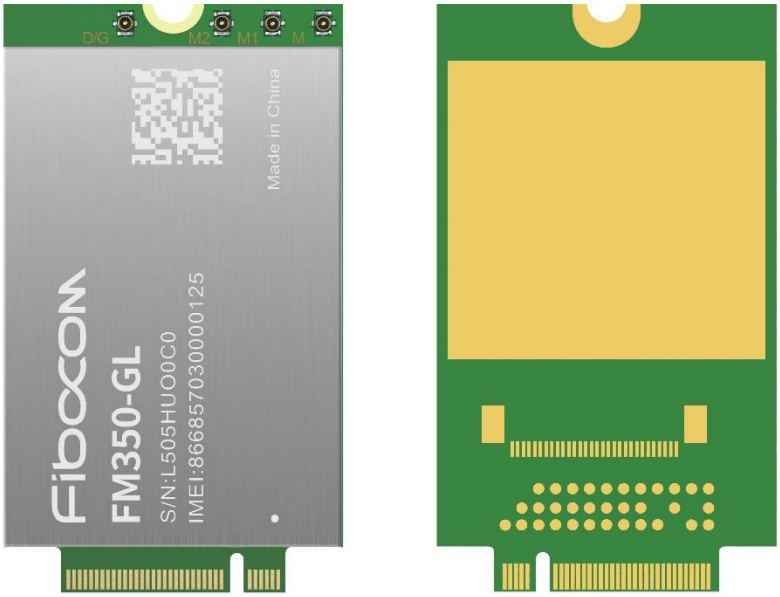

Figure 6-1 Module appearance

6.2 Dimension of Structure

The structural dimension of the FM350 module is shown in Figure 6-2:

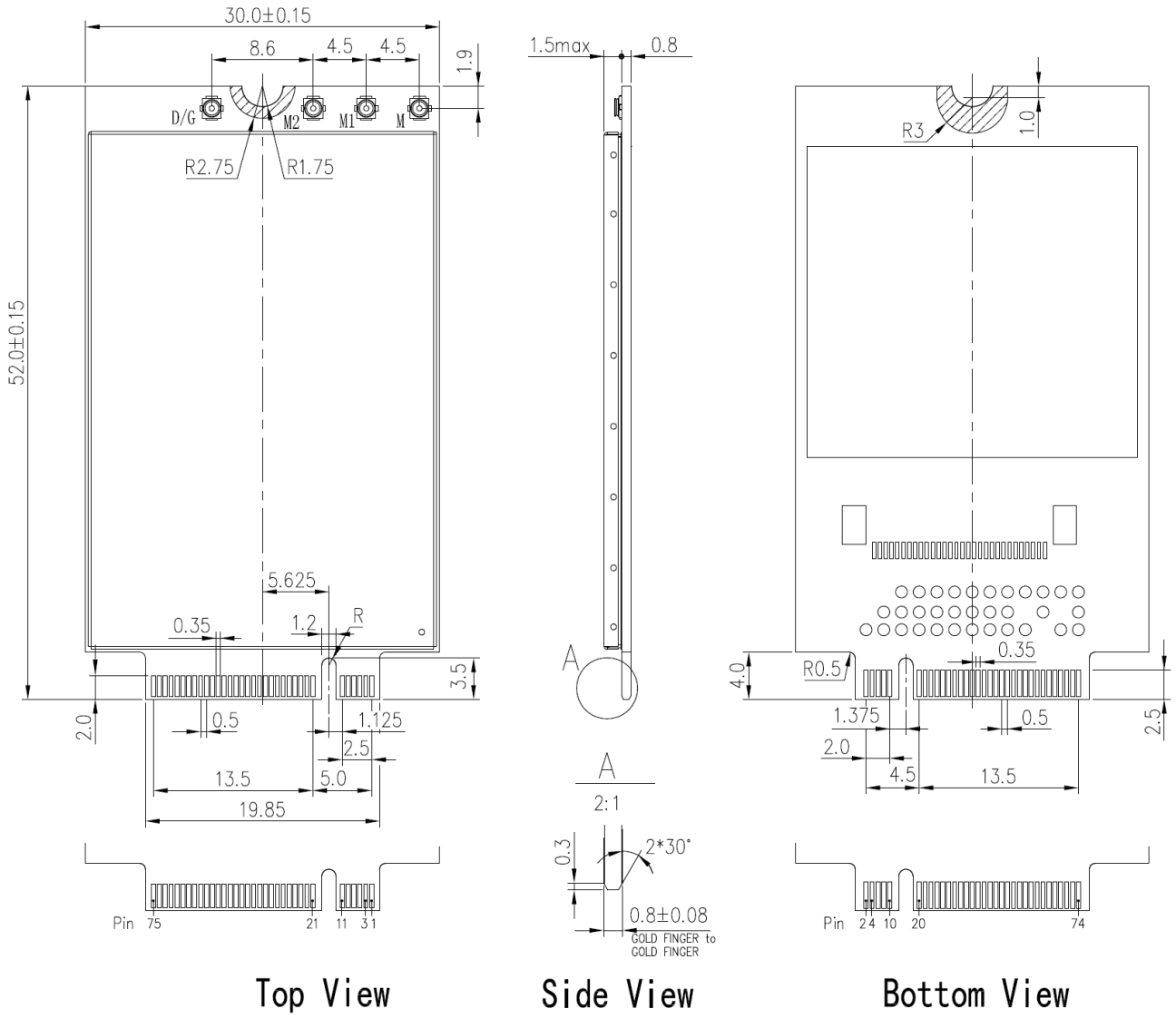

Figure 6-2 Dimension of structure (unit: mm)

6.3 M.2 Interface Model

The FM350 M.2 module adopts 75-pin gold finger as external interface, where 67 pins are signal pins and 8 pins are notch pins as shown in Figure 3-1. For module dimension, please refer to Figure 6-2 Dimension of Structure. Based on the M.2 interface definition, FM350 module adopts Type 3052-S3-B interface (30x52mm, the component maximum height on t top layer is 1.5mm, PCB thickness is 0.8mm, and KEY ID is B).

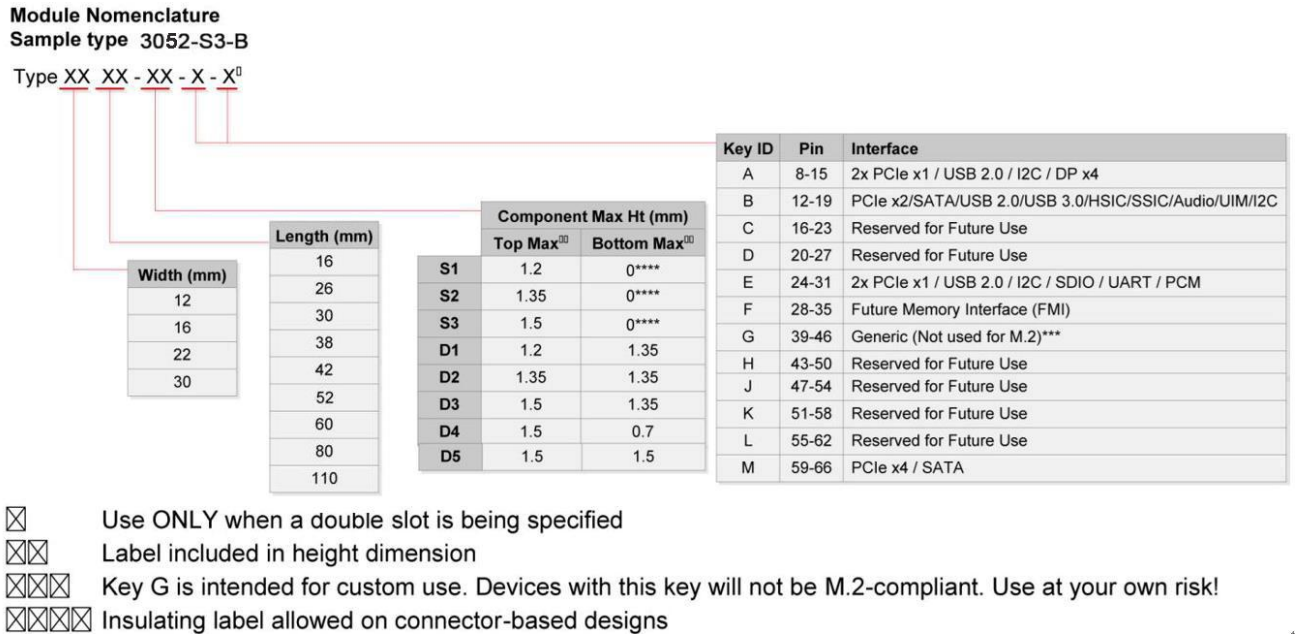

Figure 6-3 M.2 interface model

6.4 M.2 Connector

FM350 module connects with host by M.2 connector which is built in host. The recommended part number is APCI0026-P001A manufactured by LOTES Corporation, and the dimensions is shown in Figure 6-4. For stack-up top-mount single-sided module, the recommended part number is APCI0144-P001A, manufactured by LOTES Corporation, and the dimension is shown in Figure 6-5. The package of connector, please refer to the specification.

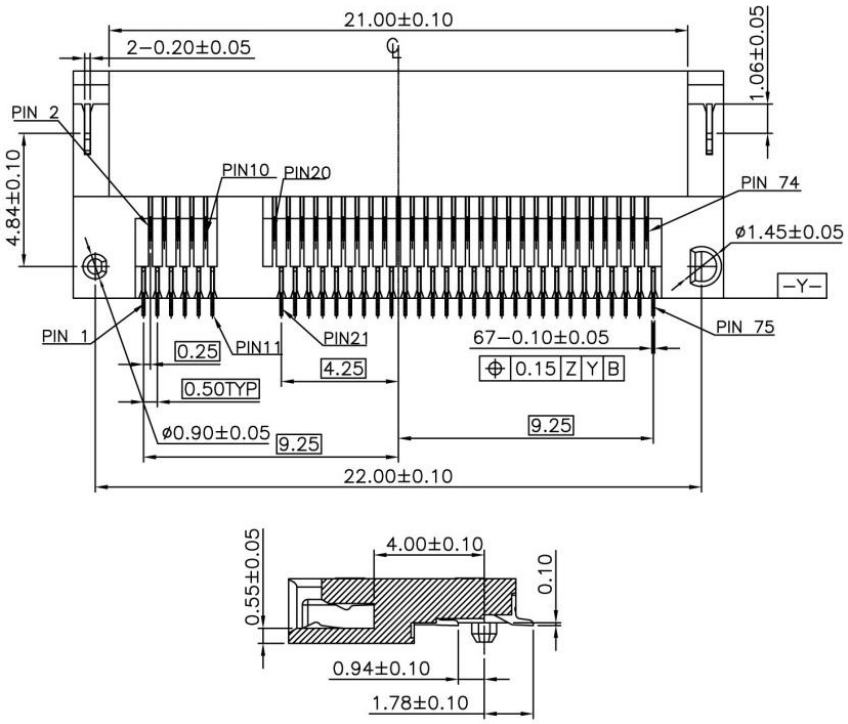

Figure 6-4 M.2 Dimension of structure for stack-up Mid-mount single-sided module

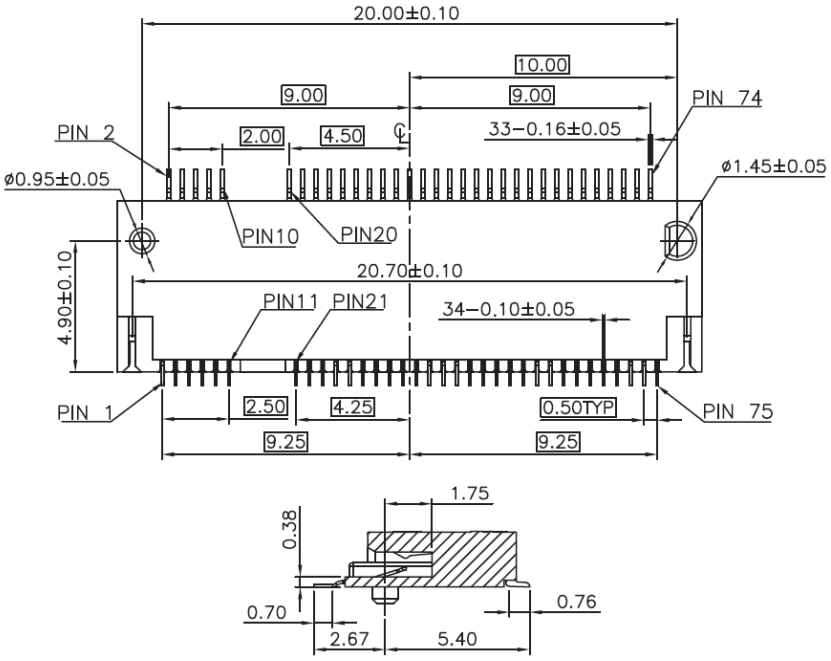

Figure 6-5 M.2 dimension of structure for stack-up top-mount single-sided module

6.5 M.2 Card Assembly

6.5.1 Card Insertion

Angled insertion is allowable and preferred; intent is to minimize the insertion and extraction force. The minimum angle of insertion is 5°. For APCI0144-P001A, the maximum angle of insertion is 5°. For APCI0026-P001A, the maximum angle of insertion is 20°. PLS refer to Figure 6-6 and Figure 6-7 to insert and extract the module.

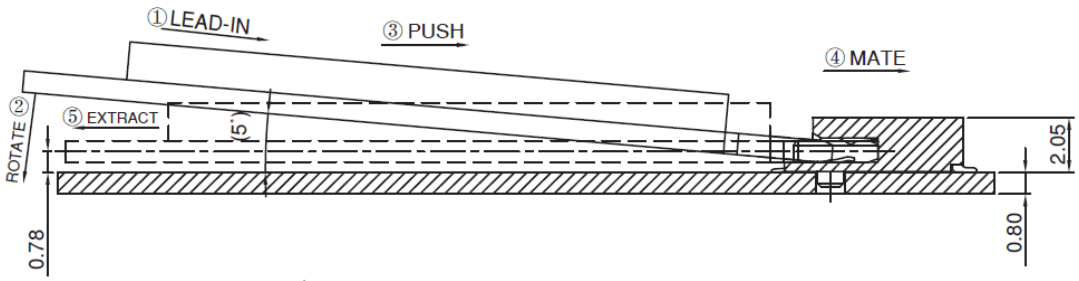

Figure 6-6 Angle of insertion for APCI0144-P001A

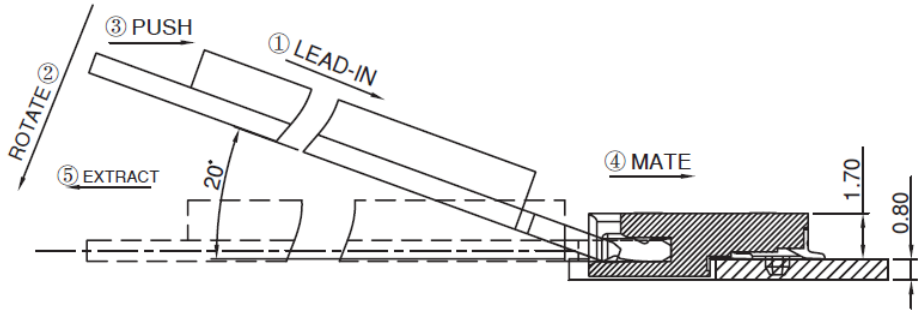

Figure 6-7 Angle of insertion for APCI0026-P001A

6.5.2 Mid-mount Connection with Single-Sided Module

Stack-up Mid-mount (In-line) single-sided module is shown in Figure 6-8. The maximum height of components is 1.5mm.

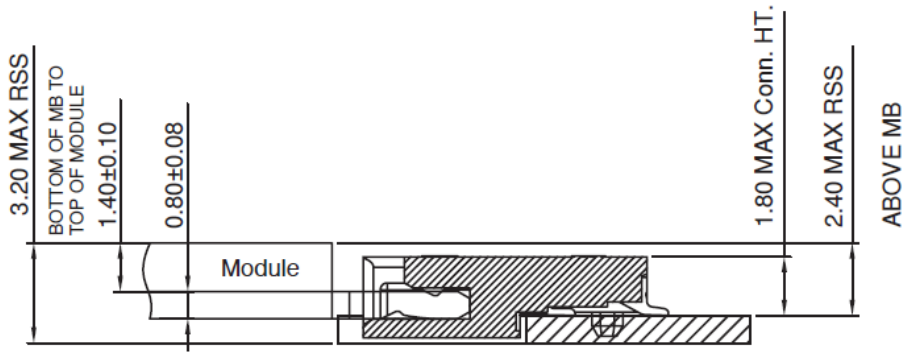

Figure 6-8 Stack-up mid-mount single-sided module

Note：

2.4mm maximum above mother board

Suggest to cut the area of mother board under M.2 module

6.5.3 Top-mount Connection with Single-Sided Module

Stack-up top-mount single-sided module is shown in Figure 6-9. The maximum height of components is 1.5mm.

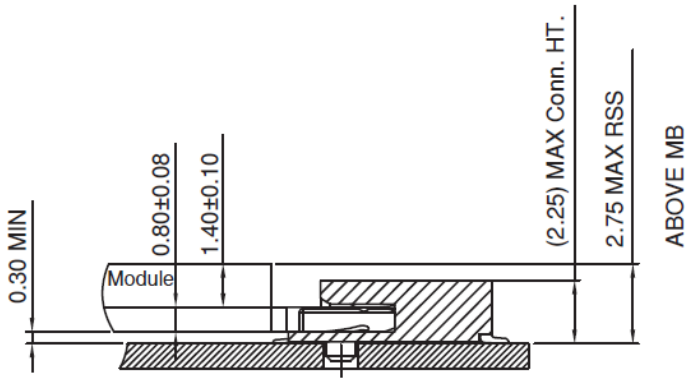

Figure 6-9 Stack-up top-mount single-sided module

Note：

2.75mm maximum above mother board

Full keep out area 30×42mm below module, which means don’t place any components and routings below M.2 module

Add thermal pad between M.2 module and mother board for thermal dissipation.

6.6 Storage

6.6.1 Storage Life

Storage Conditions (recommended): Temperature is 23 ± 5℃, relative humidity is less than RH 60%.

Storage period: Under the recommended storage conditions, the storage life is 12 months.

6.7 Packing

The FM350 module uses the tray sealed packing, combined with the outer packing method using the hard cartoon box, so that the storage, transportation and the usage of modules can be protected to the greatest extent.

Note：

The module is a precision electronic product, and may suffer permanent damage if no correct electrostatic protection measures are taken.

6.7.1 Tray Package

The FM350 module uses tray package, 20 pcs are packed in each tray, with 5 trays including one empty tray on top in each box and 5 boxes in each case. Tray packaging process is shown in Figure 6-10:

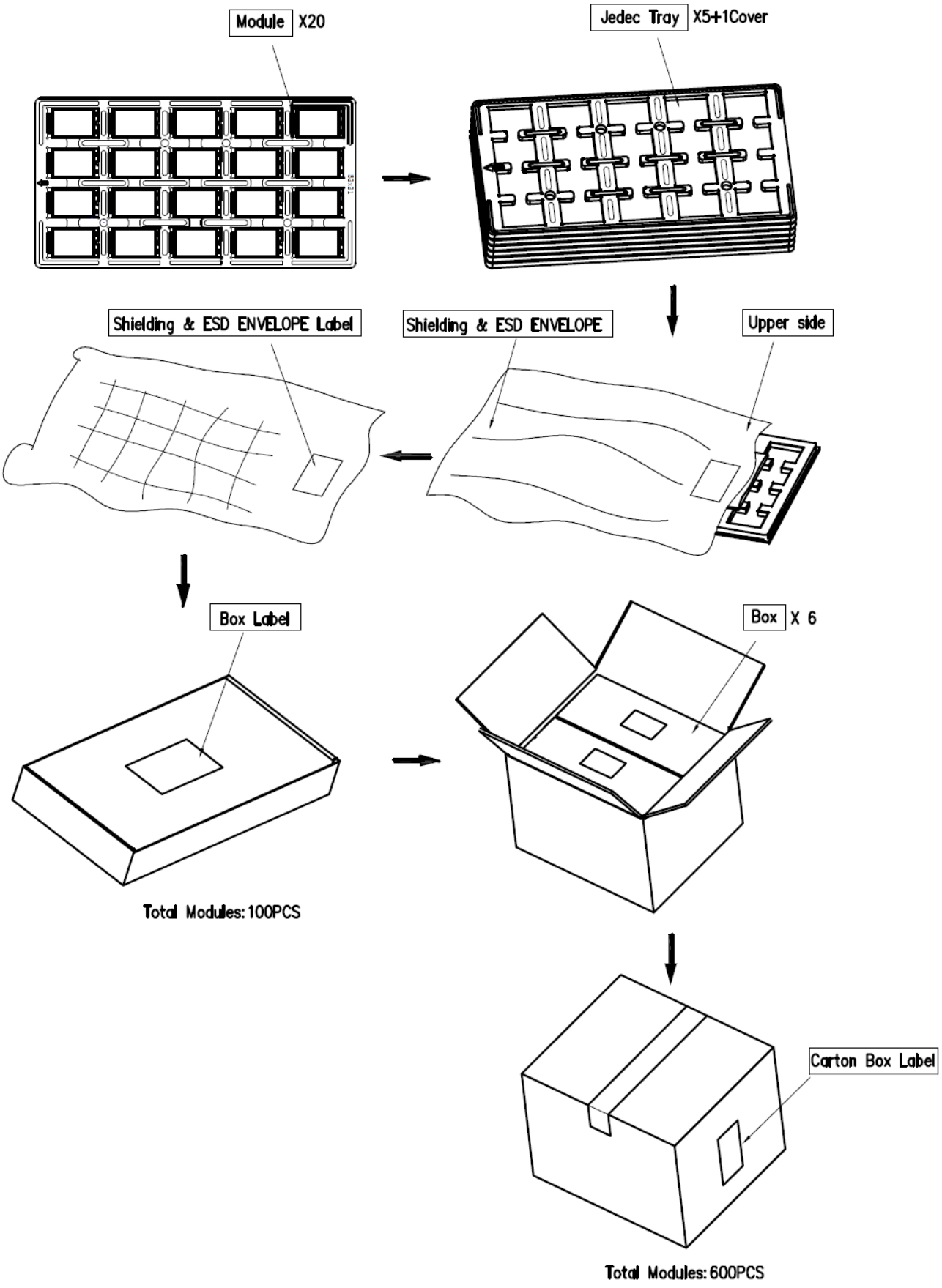

Figure 6-10 Tray packaging process

6.7.2 Tray Size

The pallet size is 330x175x6.5mm, and is shown in Figure 6-11:

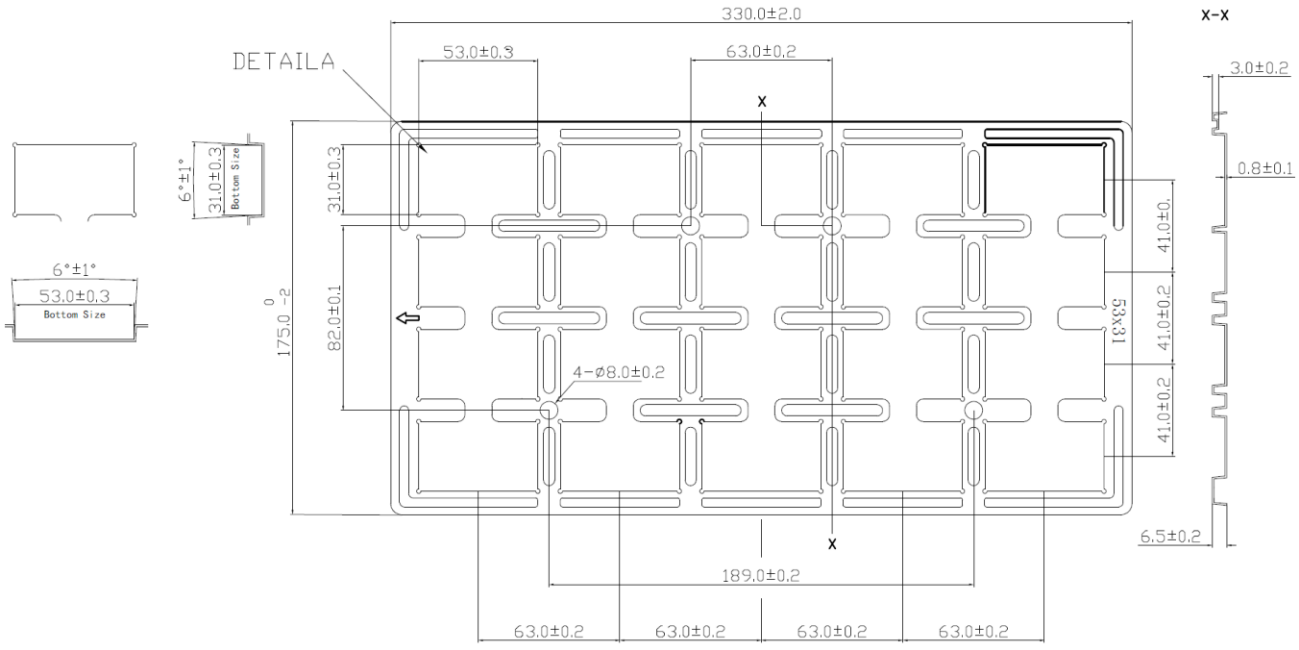

Figure 6-11 Tray size (unit: mm)